CURRICULUM VITAE

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Education

- Doctorate of Philosophy (Ph.D.) in Electrical and Computer Engineering, August 2006
  University of Arizona, Tucson.
- Master of Science (M.S.) in Electrical and Computer Engineering, May 2003
  University of Arizona, Tucson.
- Bachelor of Engineering (B.E.), Electronics and Communications, February 2000.
  Manipal Institute of Technology, Manipal, India.
  First Class with Distinction.

Employment

- ***Professor (with tenure)***, August 2016 - present,
  School of Electrical Engineering and Computer Science, Ohio University, Athens, Ohio.
- ***Associate Professor (with tenure)***, August 2012 - August 2016,
  School of Electrical Engineering and Computer Science, Ohio University, Athens, Ohio.
- *Consultant*, September 2013 - February 2017
  Advanced Micro Devices (AMD) Research, Exascale FastForward and Design Forward - 2.
- *On-Site Consultant*, February 2013 - July 2013,
  Advanced Micro Devices (AMD) Research, Exascale FastForward, Austin, Texas.
- ***Assistant Professor (on tenure-track)***, September 2007 - August 2012,
  School of Electrical Engineering and Computer Science, Ohio University, Athens, Ohio.
- *Post-Doctoral Research Associate*, August 2006 - August 2007,
  Department of Electrical and Computer Engineering, University of Arizona, Tucson, Arizona.
- *Graduate Research Associate*, August 2000 - August 2006,
  Department of Electrical and Computer Engineering, University of Arizona, Tucson, Arizona.
- *Associate Consultant*, December 1999 - July 2000
  iGATE Corporation, Bangalore, India.

Research Grants and Contracts

Secured in excess of $4.3 Million in external grants and contracts.

On-going Research Grants

1. **New** *Air Force Research Laboratory* - "ADMETE: Assured Digital Microelectronics Education & Training Ecosystem," - (Role - PI, Co-PIs are Savas Kaya, Harsha Chenji, David Juedes, Frank Drews and Chad Mourning Funded @ $486,000 from 09/03/2020 - 02/03/2023).

2. **New** *National Science Foundation* - "SaTC: CORE: Small: Language Abstractions for Reconfigurable Hardware Monitors on Manycore Architectures," - (Role - PI, Co-PI is Gordon Stewart Funded @ $499,449 from 09/2020 - 08/2023).

3. **New** *Ohio Department of Higher Education* - "Strategic Educational Initiatives to Improve Cyber-Defenses in State of Ohio," - (Role - PI, Co-PI are Savas Kaya, David Juedes, Gordon Stewart and Harsha Chenji Funded @ $225,161 from 02/2020 - 06/2021).

4. *National Science Foundation* - "SHF: Medium: Collaborative Research: Photonic Neural Network Accelerator for Energy-Efficient Heterogeneous Multicore Architectures," (Role - PI, Co-PI is Razvan Bunescu Funded @ $523,999 from 08/2019 - 07/2022).

5. *National Science Foundation* - "SHF: Medium: Collaborative Research: Machine Learning Enabled Network-on-Chip Architectures Optimized for Energy, Performance and Reliability," (Role - PI, Co-PI is Razvan Bunescu Funded @ $524,000 from 08/2017 - 07/2021).

6. *National Science Foundation* - "SHF: Medium: Collaborative Research: Scaling On-chip Networks to 1000-Core Systems using Heterogeneous Emerging Interconnect Technologies," (Role - PI, Co-PI is Savas Kaya Funded @ $496,000 from 09/2015 - 08/2021).

Completed Research Grants

1. *National Science Foundation* - "SHF: Small: Collaborative Research: A Holistic Design Methodology for Fault-Tolerant and Robust Network-on-Chips (NoCs) Architectures," (Role - PI @ $208,000 from, 09/2014 08/2019).

2. *National Science Foundation* - "**CAREER:** Design of Reconfigurable Power and Area-Efficient Nanophotonic Architectures for Future Multi-cores," (Role: PI, Funded @ $524,000, from 04/2011 - 03/2018).

3. *National Science Foundation* - "Collaborative Research: SHF: Small: Power-Efficient and Reliable 3D Stacked Reconfigurable Photonic Network-on-Chips for Scalable Multicore Architectures," (Role - PI @ $153,000 from 08/2013 - 07/2018).

4. *National Science Foundation* - "Collaborative Research: EAGER: Exploiting Heterogeneity in Emerging Interconnect Technologies for Building Highly Scalable and Power-Efficient Network-on-Chips for Multi-core Systems," (Role- PI @ $59,999 from 07/2013 - 11/2016).

5. *Advanced Micron Devices* - "Exascale Computing Systems," (Funded @ $89,912, from 02/2013 - 08/2013).

6. *National Science Foundation* - "Power-Efficient Reconfigurable Wireless Network-on-Chip (NoC) Interconnects for Future Many-core Architectures," (Role: PI, Co-PIs are Savas Kaya and David Matolak Funded @ $380,000, from 09/2011 - 08/2014).

7. *National Science Foundation* - "Collaborative Research: Design of Power and Area Efficient, Fault-tolerant Network-on-Chips (NoCs) Circuits and Architectures," (Role: PI at Ohio University, Funded @ $134,437, 09/2009 - 08/2012).

Honors and Awards

- *IEEE Transactions on Computing Award for Editorial Service and Excellence* - 2020
- *Marvin E. and Ann D. White Research Award* - Russ College of Engineering and Technology, Ohio University May 2020
- *Best Paper Candidate* - IEEE Design and Test in Europe (DATE) 2019
- **Joseph Jachinowski Professor in EECS** - 2018
- *Presidential Research Scholar Award* - 2017
- *Marvin E. and Ann D. White Research Award* - Russ College of Engineering and Technology, Ohio University May 2014
- *Best Paper Award* - 31st IEEE Conference on Computer Design, October 2013.
- *Marvin E. and Ann D. White Research Award* - Russ College of Engineering and Technology, Ohio University May 2012
- *Outstanding Research Paper Award* - Russ College of Engineering and Technology, Ohio University May 2011.
- *NSF CAREER Award* - 2011
- *Best Paper Candidate* - 4th ACM/IEEE International Symposium on Network-on-Chips, May 2010 - (Selected 4/27 Accepted Papers)
- *Best Paper Candidate* - 14th Asia and South Pacific Design Automation Conference, Jan 2009 - (Selected 12/116 Accepted Papers)
- *Top Picks in IEEE Micro Magazine* - from IEEE Hot Interconnects Symposium'03, Jan 2004.
- *First Class with Distinction* - Graduated Bachelor of Engineering in Electronics and Communications, Feb 2000.

Research Interests

- Computer Architecture.
- Network-on-Chips (NoCs).
- Emerging Technologies (Nanophotonics, Wireless and 3D Stacking).
- Hardware Accelerators and Machine Learning.
- Hardware Security.

Publications

Book Chapters

1. Avinash Karanth Kodi, Randy Morris and Ahmed Louri, "Scalable 3D Optical Interconnects for Data Centers," **Elseiver Publishing**, Optical Interconnects for Data Centers, 2016.

2. Avinash Karanth Kodi and Ahmed Louri, "Optical Interconnection Network for High-Performance Parallel Computers," **Research Signpost**, Recent Research Development in Optics, vol.4, Trivandrum, India, 2004.

Peer-Reviewed Journal Articles

1. Quintin Fettes, Avinash Karanth, Razvan Bunescu, Ahmed Louri and Kyle Shiflett, "Hardware-based Thread Migration to Reduce On-Chip Data Movement with Reinforcement Learning," **IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)**, vol. 39, no. 11, pp. 3638-3649, November 2020.

2. Xuehai Qian, Yanzhi Wang and Avinash Karanth, "Guest Editors' Introduction to the Special Issue on Machine Learning Architectures and Accelerators," **IEEE Transactions on Computers (TC)**, vol. 69, no. 7, pp. 929-930, July 2020.

3. Talha Canan, Savas Kaya, Avinash Karanth, and Ahmed Louri, "Ultra-Compact and Low-Power Logic Circuits via Work-Function Engineering," **IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JXCDC)**, vol. 5, no. 2, pp. 94-102, December 2019.

4. Avinash Karanth, Savas Kaya, Ashif Sikder, Daniel Carbaugh, Soumyasanta Laha, Ahmed Louri, Hao Xin, Junqiang Wu and Dominic DiTomaso, "Sustainability in Network-on-Chips by Exploring Heterogeneity in Emerging Technologies," **IEEE Transactions on Sustainable Computing (TSUSC)**, vol. 4, no. 3, pp. 293-307, July/September 2019.

5. Quintin Fettes, Mark Clark, Razvan Bunescu, Avinash Karanth, and Ahmed Louri, "Dynamic Voltage and Frequency Scaling in NoCs with Supervised and Reinforcement Learning Techniques," **IEEE Transactions on Computers (TC)**, vol. 68, no. 3, pp. 375-389, March 2019.

6. Ahmed Louri, Jacques Collet and Avinash Karanth, "Limit of Hardware Solutions for Self-Protecting Fault-Tolerant NoCs," **ACM Journal on Emerging Technologies for Computing Systems (JETC)**, vol. 15, no. 1, February 2019.

7. Talha Canan, Savas Kaya, Avinash Karanth, Ahmed Louri and Hao Xin, "Ambipolar SB-FinFETs: A New Path to Ultra-Compact sub-10nm Logic Circuits," **IEEE Transactions on Electron Devices (TED)**, vol. 66, no. 1, pp. 255-263, January 2019.

8. Seaghan Sefton, Taiman Siddiqui, Nathaniel St. Armour, Gordon Stewart and Avinash Kodi, "GARUDA: Designing Energy-Efficient Hardware Monitors from High-Level Policies for Secure Information Flow," **IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)**, vol. 37, no. 11, pp. 2509-2518, November 2018.

9. Scott VanWinkle and Avinash Kodi, "SHARP: Shared Heterogeneous Architecture with Reconfigurable Photonic Network-on-Chip," **ACM Journal on Emerging Technologies in Computing Systems (JETC)**, Special Issue on Silicon Photonics, vol. 14, no. 2, July 2018.

10. Travis Boraten and Avinash Kodi, "Runtime Fault Tolerant Techniques to Mitigate Soft Errors in Network-on-Chips (NoCs) Architectures," **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems**, vol. 37, no. 3, pp. 682-695, March 2018.

11. Travis Boraten and Avinash Kodi, "Mitigation of Hardware Trojan based Denial-of-Service Attack for Secure NoCs," Elsevier **Journal of Parallel and Distributed Computing (JPDC)**, vol. 111, pp. 24-38, January 2018.

12. Junqiang Wu, Avinash Kodi, Savas Kaya, Ahmed Louri and Hao Xin, Monopoles Loaded with 3D-Printed Dielectrics for Future Wireless Intra-Chip Communications, **IEEE Transactions on Antennas and Propagation**, vol. 65, no. 12, pp. 6838-6846, December 2017.

13. Matthew Kennedy and Avinash Kodi, "Laser Pooling: Static and Dynamic Laser Power Allocation for On-Chip Optical Interconnects," **IEEE/OSA Journal of Lightwave Technology (JLT)**, Special Issue on Optical Interconnects Conference, vol. 35, no. 15, pp. 3159-3167, Aug 2017.

14. William Rayess, David Matolak, Savas Kaya and Avinash Karanth Kodi, "Antennas and Channel Characteristics for Wireless Networks on Chips," **Wireless Personal Communications**, pp. 1-18, April 2017.

15. Matthew Kennedy and Avinash Kodi, "CLAP-NET: Bandwidth Adaptive and Power Regulated Optical Crossbar Architecture," **Journal of Parallel and Distributed Systems (JPDC)**, vol. 100, pp. 130-139, February 2017.

16. Dominic DiTomaso, Avinash Kodi, Ahmed Louri and Razvan Bunescu, "Resilient and Power-Efficient Multi-Function Channel Buffers in Network-on-Chip Architectures," **IEEE Transactions on Computers**, vol. 64, no. 12, pp. 3555-3568, December 2015.

17. Dominic DiTomaso, Avinash Kodi, David Matolak, Savas Kaya, Soumyasanta Laha and William Rayess, "A-WiNoC: Adaptive Wireless Network-on-Chips (NoCs) Architecture for Future Multicores ," **IEEE Transactions on Parallel and Distributed Systems (TPDS)**, vol. 26, no. 12, pp. 3289-3302, December 2015.

18. Soumyasanta Laha, Savas Kaya, David W. Matolak, William Rayess, Dominic DiTomaso and Avinash Kodi, "A New Frontier in Ultra-low Power Wireless Links: Network-on-Chip and Chip-to-Chip Interconnects," **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)**, vol. 34, no. 2, pp. 186-198, February 2015.

19. Avinash Kodi, Brian Neel and William C. Brantley, "Photonic Interconnects for Exascale and Datacenter Architectures," **IEEE Micro**, Special Issue on Novel Architectures for High-Speed Data Center Interconnects, vol. 34, no. 5, pp. 18-30, September/October 2014.

20. Randy Morris, Avinash Kodi, Ahmed Louri and Ralph Whaley, "3D Stacked Nanophotonic Architecture with Minimal Reconfiguration," **IEEE Transactions on Computers**, vol. 63, no. 1, pp. 243-255, January 2014.

21. Randy Morris, Evan Jolley and Avinash Kodi, "Extending the Performance and Energy-Efficiency of Nanophotonic Interconnects for Shared Memory Multicores," **IEEE Transactions on Parallel and Distributed Systems**, vol. 25, no. 1, pp. 83-93, January 2014.

22. Jin Sun, Roman Lysecky, Karthik Shankar, Avinash Kodi, Ahmed Louri and Janet Wang, "Workload Assignment Considering NBTI Degradation in Multi-core Systems," **ACM Journal on Emerging Technologies in Computing Systems (JETC)**, vol. 10, no. 1, pp. 1-22, January 2014.

23. Dominic DiTomaso, Randy Morris, Avinash Kodi, Ashwini Sarathy and Ahmed Louri, "Extending the Energy-Efficiency and Performance with Channel Buffers, Crossbars and Topology Analysis for NoCs," **IEEE Transactions on VLSI (TVLSI)**, vol. 21, no. 11, pp. 2141 - 2154, November 2013.

24. David W. Matolak, Savas Kaya, and Avinash Kodi, Channel Modeling for Wireless Networks-on-Chips, **IEEE Wireless Communications Magazine**, vol. 51, no. 6, pp. 180-186, June 2013.

25. David W. Matolak, Avinash Kodi, Savas Kaya, Dominic DiTomaso, Soumyasanta Laha and William Rayess, "Wireless Networks-on-Chips: Architecture, Wireless Channel, and Devices," **IEEE Wireless Communications Magazine**, Special Issue on Wireless Communication at Nanoscale, vol. 19, no. 5, pp. 58-65, October 2012.

26. Brian Neel, Randy Morris, Dominic DiTomaso and Avinash Kodi, "SPRINT: Scalable Photonic Switching Fabric for High-Performance Computing (HPC)," **OSA/IEEE Journal of Optical Communications and Networking (JOCN)**, Special Issue on Enabling Optical Devices for Scalable Networks, vol. 4, no. 9, A37-A48, September 2012.

27. Ahmed Louri and Avinash Karanth Kodi, "Introduction to the Special Issue on Networks-on-Chip (NoC) in Journal of Parallel and Distributed Systems (JPDC)," in **Journal of Parallel and Distributed Systems**, vol. 71, issue 5, pp. 623-624, May 2011.

28. **(invited)** Avinash Karanth Kodi and Ahmed Louri, "Energy Efficient and Bandwidth Reconfigurable Photonic Networks for High-Performance Computing (HPC) Systems," in **IEEE Journal of Selected Topics in Quantum Electronics**, Special Issue on Green Photonics, vol. 17, no. 2, pp.384-395, March/April 2011.

29. Yixuan Zhang, Randy Morris and Avinash Karanth Kodi, "Design of a Power-Efficient Dual-Crossbar Network-on-Chip Architecture," **Elseiver Microprocessors and Microsystems, Embedded Hardware Design**, (Special Issue on NoCs), vol. 35, pp. 110-118, March 2011.

30. Ahmed Louri and Avinash Karanth Kodi, "Special Issue on Network-on-Chips (NoCs)," **Journal of Parallel and Distributed Computing**, vol. 70, issue 1, pp. 90, December 2010.

31. Randy Morris and Avinash Karanth Kodi, "Exploring the Design of 64 & 256 core Power Efficient Nanophotonic Interconnect ," **IEEE Journal of Selected Topics in Quantum Electronics**, vol. 16, no. 5, pp. 1386-1393, September/October 2010.

32. Avinash Karanth Kodi and Ahmed Louri, "Multi-dimension and Reconfigurable Optical Interconnects for High-Performance Computing (HPC) Systems," **IEEE Journal of Lightwave Technology**, vol. 27, no. 21, pp. 4634-4641, November 2009.

33. Avinash Karanth Kodi and Ahmed Louri, "Reconfigurable and Adaptive Photonic Networks for High-Performance Computing (HPC) Systems," **OSA Applied Optics**, Special Issue on Optical High-Performance Computing, vol. 48, no. 22, pp. E13-E23, August 2009.

34. Avinash Karanth Kodi and Ahmed Louri, "OPTISIM: A System Simulation Methodology for Optically Interconnected High-Performance Computing Systems," **IEEE Micro**, vol. 28, no. 5, pp. 22-36, September/October 2008.

35. Avinash Karanth Kodi, Ashwini Sarathy, and Ahmed Louri, "Adaptive Channel Buffers in On-Chip Interconnection Networks - A Power and Performance Analysis," **IEEE Transactions on Computers**, vol. 57, no. 9, pp. 1169-1181, September 2008.

36. Ashwini Sarathy, Avinash Karanth Kodi and Ahmed Louri, "Low-Power Low-Area Network-on-Chip Architecture using Adaptive Channel Buffers," **IEE Electronics Letters**, vol. 44, no. 8, pp. 512-513, April 10, 2008.

37. Avinash Karanth Kodi and Ahmed Louri, "A System Simulation Methodology of Optical Interconnects for High-Performance Computing (HPC) Systems," **OSA Journal of Optical Networking**, vol.6, no.12, pp. 1282-1300, December 2007.

38. Chander Kochar, Avinash Karanth Kodi, and Ahmed Louri, "Proposed Low-Power High-Speed Microring Resonator-based Switching Technique for Dynamically Reconfigurable Optical Interconnects," **IEEE Photonics Technology Letters**, vol. 19, no. 17, pp. 1304-1306, September 2007.

39. Chander Kochar, Avinash Karanth Kodi, and Ahmed Louri, "nD-RAPID: A Multi-Dimension Scalable Fault-tolerant Opto-Electronic Interconnection for Scalable High-Performance Computing Systems," **OSA Journal of Optical Networking**, Special Issue on Photonics in Switching, vol.6, no.5, pp. 465-481, May 2007.

40. Avinash Karanth Kodi and Ahmed Louri, "RAPID for High-Performance Computing: Architecture and Performance Evaluation," **OSA Applied Optics**, Special Issue on Information Photonics, vol. 45, no. 25, pp. 6326-6334, September 2006.

41. Avinash Karanth Kodi and Ahmed Louri, "Design of High-Speed Optical Interconnect for Scalable Shared Memory Multiprocessors," **IEEE Micro**, Special Issue on Hot Interconnects, vol. 25, no. 1, pp. 41-49, Jan/Feb 2005.

42. Ahmed Louri and Avinash Karanth Kodi, "An Optical interconnection network and a modified snooping protocol for the design of Large-scale Symmetric Multiprocessors (SMPs)", **IEEE Transactions on Parallel and Distributed Systems**, vol. 15, no. 12, pp. 1093-1104, December 2004.

43. Avinash Karanth Kodi and Ahmed Louri, "RAPID: Reconfigurable and scalable All-Photonic Interconnect for Distributed shared memory multiprocessors", **IEEE/OSA Journal of Lightwave Technology**, Special Issue on Optical Interconnects, vol. 22, no. 9, pp. 2101-2110, September 2004.

44. Ahmed Louri and Avinash Karanth Kodi, "SYMNET: An Optical Interconnection Network for Large-scale, High-Performance Symmetric Multiprocessors," **OSA Applied Optics**, vol. 42, no. 17, pp 3407-3417, June 10, 2003.

45. Ahmed Louri and Avinash Karanth Kodi, "Parallel Optical Interconnection Network for Address Transactions in Large-scale, Cache coherent Symmetric Multiprocessors (SMPs)", **IEEE Journal of Selected Topics in Quantum Electronics**, Special Issue on Optical Interconnects, vol.9, no.2, pp. 667-676, March/April 2003.

46. Ahmed Louri and Avinash Karanth Kodi, "Scalable Optical Interconnection Networks for Symmetric Multiprocessors (SMPs)," in **Optics in Information Systems, SPIE's International Technical Group Newsletter**, vol. 14, no. 1, March 2003.

Peer Reviewed Conference and Workshop Papers

47. Kyle Shiflett, Avinash Karanth, Ahmed Louri, and Razvan Bunescu, "Albireo: Energy-Efficient Acceleration of Convolutional Neural Networks via Silicon Photonics," Accepted to appear in *48th IEEE International Symposium on Computer Architecture (ISCA)*, June 14-19, 2021. (Acceptance Rate $\sim$ 18% (=76/406))

48. Kyle Shiflett, Avinash Karanth, Ahmed Louri, and Razvan Bunescu, "Bitwise Neural Network Acceleration Using Silicon Photonics," Accepted to appear in *31st ACM Great Lakes Symposium on VLSI*, June 22-25, 2021.

49. Yuan Li, Ahmed Louri and Avinash Karanth, "Scaling Deep Learning Inference with Chiplet-based Architecture and Photonic Interconnects, Accepted to appear in *Design Automation Conference (DAC)*, San Francisco, CA, July 11-15, 2021.

50. Jiajun Li, Ahmed Louri, Avinash Karanth and Razvan Bunescu, "CSCNN: Algorithm-hardware Co-design for CNN Accelerators using Centrosymmetric Filters," Accepted to appear in *27th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Seoul, South Korea, Feb 27 - March 3, 2021.

51. Jiajun Li, Ahmed Louri, Avinash Karanth and Razvan Bunescu, "GCNAX: A Flexible Dataflow Accelerator for Graph Convolution Neural Networks," Accepted to appear in *27th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Seoul, South Korea, Feb 27 - March 3, 2021.

52. Kyle Shiflett, Avinash Karanth, Ahmed Louri and Razvan Bunescu, Energy-Efficient Multiply-and-Accumulate using Silicon Photonics for Deep Neural Network, *IEEE Photonics Conference (IPC)*, Vancouver, Canada, Sept 27 Oct 1, 2020.

53. Talha Canan, Savas Kaya, Harsha Chenji and Avinash Karanth, "Reconfigurable Gates with Sub-10nm Ambipolar SB-FinFETs for Logic Locking & Obfuscation," *63rd IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, Springfield, MA, August 9-12 2020.

54. Mark Clark, Yingping Chen, Avinash Karanth, Brian Ma and Ahmed Louri, "DoZZNoC: Reducing Static and Dynamic Energy in NoCs with Low-Latency Voltage Regulators using Machine Learning," *26th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2020)*, New Orleans, LA, May 18-22, 2020.

55. Kyle Shiflett, Dylan Wright, Avinash Karanth and Ahmed Louri, "PIXEL: Photonic Neural Network Accelerator," *26th IEEE International Symposium on High-Performance Computer Architecture (HPCA 2020)*, San Diego, CA, February 22-26, 2020. (Acceptance Rate $\sim$ 48/248 = 19%)

56. Ke Wang, Ahmed Louri, Avinash Karanth and Razvan Bunescu, "IntelliNoC: A Holistic Framework for Energy-Efficient and Reliable On-Chip Communication for Manycores," *46th IEEE International Symposium on Computer Architecture (ISCA)*, Phoenix, AZ, June 22-26, 2019. (Acceptance Rate $\sim$ 17%)

57. Ke Wang, Ahmed Louri, Avinash Karanth and Razvan Bunescu, "High-Performance, Energy-Efficient, and Fault-Tolerant Network-on-Chip Design using Reinforcement Learning," *IEEE Design and Test in Europe (DATE)*, Florence, Italy, March 24-28, 2019. (Acceptance Rate $\sim$ 24%)

58. Talha Canan, Savas Kaya, Avinash Karanth, Ahmed Louri and Hao Xin, "10T and 8T Full Adders Based on Ambipolar XOR Gates with SB-FinFETs," *2018 IEEE International Conference on Electronics, Circuits & Systems (ICECS)*, Bordeaux, France, Dec 9-12, 2018.

59. Padmaja Bhamidipati and Avinash Karanth, "RETUNES: Reliable and Energy-Efficient Network-on-Chip Architecture," *36th IEEE International Conference on Computer Design (ICCD)*, Orlando, FL, Oct 7-10, 2018. (Acceptance Rate $\sim$ 29%)

60. Seaghan Sefton, Taiman Siddiqui, Nathaniel St. Armour, Gordon Stewart and Avinash Kodi, "GARUDA: Designing Energy-Efficient Hardware Monitors from High-Level Policies for Secure Information Flow," *IEEE/ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, Torino, Italy, September 30 - October 5, 2018.

61. Travis Boraten and Avinash Kodi, "Securing NoCs Against Timing Attacks with Non-Interference Based Adaptive Routing," *12th IEEE/ACM International Symposium on Network-on-Chips (NoCs)*, Torino, Italy, October 4-5, 2018.

62. Talha Canan, Savas Kaya, Avinash Karanth Kodi, Ahmed Louri and Hao Xin, "Sub-THz Tunable Push Push Oscillators with FinFETs for Wireless NoCs," *61st IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, Windsor, ON, Canada, August 5-8, 2018.

63. Mark Clark, Avinash Kodi, Razvan Bunescu and Ahmed Louri, "LEAD: Learning-enabled Energy-Aware Dynamic Voltage/Frequency Scaling in NoCs," *55th Design Automation Conference (DAC)*, San Fransisco, CA, June 24-28, 2018. (Acceptance Rate $\sim$ 24%)

64. Avinash Kodi, Kyle Shifflet, Savas Kaya, Soumyasanta Laha and Ahmed Louri, "Power-Efficient Kilo-Core Photonic-Wireless Hybrid NoCs," *32nd IEEE International Parallel and Distributed Processing (IPDPS-18)*, Vancouver, Canada, May 21-25, 2018. (Acceptance Rate $\sim$ 24.5%)

65. Scott VanWinkle, Avinash Kodi, Razvan Bunescu and Ahmed Louri, "Extending the Power-Efficiency and Performance of Photonic Interconnects for Heterogeneous Multicores with Machine Learning," *24th IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Vienna, Austria, February 24-28, 2018. (Acceptance Rate $\sim$ 20%)

66. Yashika Sharma, Junqiang Wu, Adnan Kantemur, Jinpil Tak, Avinash Kodi, Savas Kaya, Ahmed Louri and Hao Xin, "Reconfigurable Intra-Chip Antenna for Future Wireless Communications," Proceedings of 2018 USNC-URSI, Boulder, CO, January 4-8, 2018.

67. Talha Furkan Canan, Savas Kaya, Avinash Kodi, Hao Xin and Ahmed Louri, "Ultra-Compact sub-10nm Logic Circuits Based on Ambipolar SB-FinFETs," *60th IEEE International Midwest Symposium on Circuits and Systems*, Boston, MA, August 6-9, 2017.

68. Yunus Kelestemur, Soumyasanta Laha, Savas Kaya, Avinash Kodi, Hao Xin, and Ahmed Louri, "mm-Wave Tunable Colpitts Oscillators Based on FinFETs," *IEEE Wireless and Microwave Technology Conference (WAMICON)*, Cocoa Beach, FL, April 24-25, 2017.

69. Dominic DiTomaso, Ashif Sikder, Avinash Kodi and Ahmed Louri, "Machine Learning Enabled Power-Aware Network-on-Chip Design," *IEEE/ACM Design Automation and Test in Europe (DATE-17)*, Lausanne, Switzerland, March 27-31, 2017. (Acceptance Rate $\sim$ 24%)

70. Dominic DiTomaso, Travis Boraten, Avinash Kodi and Ahmed Louri, "Dynamic Error Mitigation in NoCs using Intelligent Prediction Techniques," *IEEE/ACM International Conference on Microarchitecture (MICRO-49)*, Taipei, Taiwan, October 15-19, 2016. (Acceptance Rate $\sim$ 21%)

71. Ashif Sikder, Avinash Kodi and Ahmed Louri, "R-OWN: Reconfigurable Optical Wireless NoC Architectures," *3rd ACM International Conference on Nanoscale Computing and Communication (NanoCom)*, New York, NY, September 28-29, 2016.

72. Juman Alshraiedeh and Avinash Kodi, "An Adaptive Routing Algorithm to Improve Lifetime Reliability in NoC Architectures," *IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Symposium (DFT)*, Storrs, CT, September 19-20, 2016.

73. Ashif Sikder, Avinash Kodi, Savas Kaya, David Matolak, William Rayess and Dominic DiTomaso, "Exploring Off-Chip Wireless Interconnects for DRAM Architectures," *24th Annual Symposium on High-Performance Interconnects (Hot Interconnects)*, Santa Clara, CA, August 24-25, 2016.

74. Travis Boraten and Avinash Kodi, "Mitigation of Denial of Service Hardware Trojan Attack in NoC Architectures," *International Parallel and Distributed Processing Symposium (IPDPS-16)*, Chicago, IL, May 23-27, 2016. (Acceptance Rate $\sim$ 23%)

75. Travis Boraten and Avinash Kodi, "Secure Model Checkers for Network-on-Chip (NoC) Architectures," *26th ACM's Great Lakes Symposium on VLSI (GLSVLSI-16)*, Boston, MA, May 18-20, 2016.

76. Matthew Kennedy and Avinash Kodi, "On Demand Laser Power Allocation for On-Chip Optical Interconnects," *Optical Interconnects Conference (OIC)*, San Diego, CA, May 9-11, 2016.

77. Scott VanWinkle, Matthew Kennedy, Dominic DiTomaso and Avinash Kodi, "Energy Efficient Optical Network-on-Chip Architecture for Heterogeneous Multicores," *Optical Interconnects Conference (OIC)*, San Diego, CA, May 9-11, 2016.

78. Travis Boraten and Avinash Kodi, "Packet Security with Path Sensitization in NoCs," *Design and Test in Europe (DATE-16)*, Dresden, Germany, March 14-18, 2016. (Acceptance Rate $\sim$ 24%)

79. Avinash Kodi, Brian Neel and Bill Brantley, "Power and Performance Evaluation of Exascale Architecture using Photonics," *6th IEEE International Green and Sustainable Computing Conference (IGSC-15)*, Las Vegas, NV, Dec 14-16, 2015.

80. Matthew Kennedy and Avinash Kodi, "Cross-Chip: Low Power Processor-to-Memory Nanophotonic Interconnect Architecture," *Workshop on Energy-Efficient Networks of Computers (E2NC)* held in conjunction with (IGSC-15), Las Vegas, NV, Dec 14-16, 2015.

81. Ashif Sikdar, Matthew Kennedy, Avinash Kodi, Savas Kaya and Ahmed Louri, "OWN: Optical Wireless Network-on-Chips (NoCs) for Kilo-Core Architectures," *23rd Annual Symposium on High-Performance Interconnects (Hot Interconnects)*, Santa Clara, CA, August 26-28, 2015. (Acceptance Rate $\sim$ 35%)

82. Avinash Kodi, Ashif Sikdar, Dominic DiTomaso, David W. Matolak, Savas Kaya, Soumyasanta Laha and William Rayess, "Kilocore Wireless Network-on-Chips Architectures," *2nd ACM International Conference on Nanoscale Computing and Communication (NanoCom)*, Boston, Massachusetts, September 21-22, 2015.

83. Matthew Kennedy and Avinash Kodi, "Runtime Power Reduction Techniques in On-Chip Photonic Interconnects," *25th ACM's Great Lakes VLSI Symposium (GLSVLSI)*, Pittsburgh, Pennsylvania, May 20-22, 2015. (Acceptance Rate $\sim$ 28%)

84. Matthew Kennedy and Avinash Kodi, "Design of Bandwidth Adaptive Nanophotonic Crossbars with Clockwise/Counter-Clockwise Optical Routing," *28th International Conference on VLSI Design*, Bangalore, India, January 3-7, 2015.

85. Soumyasantha Laha, Savas Kaya, Avinash Kodi and David Matolak, "LC Oscillators for Nanoscale DG-MOSFETs," *15th Annual IEEE Wireless and Microwave Technology Conference*, Tampa, Florida, June 6, 2014.

86. Dominic DiTomaso, Avinash Kodi and Ahmed Louri, "QORE: A Fault-Tolerant Network-on-Chip Architecture with Power-Efficient Quad Function Channel (QFC) Buffers," *IEEE/ACM International Symposium on High-Performance Computer Architecture (HPCA)*, Orlando, FL, Feb 15-19, 2014. (Acceptance Rate $\sim$ 25%)

87. Travis Boraten and Avinash Kodi, "Runtime Adaptive Scrubbing for Fault-Tolerant Networks-on-Chips (NoCs) Architectures," *31st IEEE International Conference on Computer Design (ICCD)*, Ashville, NC, Oct 6-9, 2013. (Acceptance Rate $\sim$ 25%, **BEST PAPER**)

88. Savas Kaya, Soumyasanta Saha, Dominic DiTomaso, Avinash Kodi, David W. Matolak, and William Rayess, "On Ultra-Short Wireless Interconnects for NoCs and SoCs: Bridging the 'THz' Gap," *56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, Columbus, Ohio, August 4-7, 2013.

89. Randy Morris, Avinash Kodi and Ahmed Louri, "Evaluating the Scalability and Performance of 3D Stacked Reconfigurable Nanophotonic Interconnects," *15th IEEE/ACM System Level Interconnect Prediction (SLIP)* colocated with Design Automation Conference (DAC), Austin, TX, June 2, 2013.

90. Dominic DiTomaso, Randy Morris, Evan Jolley, Ashwini Sarathy, Ahmed Louri and Avinash Karanth Kodi, "Energy-Efficient, Fault-Tolerant Unified Buffer and Bufferless Crossbar Architecture for NoCs," *Workshop on High-Performance Power-Aware Computing (HPPAC)*, held in conjuction with IPDPS'13, Boston, Massachusetts, May 20-24, 2013.

91. Dominic DiTomaso, Avinash Kodi, David Matolak, Savas Kaya, Soumyasanta Laha and William Rayess, "Energy-Efficient Adaptive Wireless NoCs Architecture," *IEEE/ACM 7th International Symposium on Networks-on-Chips (NoCs)*, Tempe, Arizona, April 21-24, 2013. (Acceptance Rate $\sim$ 25%)

92. Li Zhou and Avinash Kodi, "PROBE: Prediction-Based Optical Bandwidth Scaling for Energy-Efficient NoCs," *IEEE/ACM 7th International Symposium on Networks-on-Chips (NoCs)*, Tempe, Arizona, April 21-24, 2013. (Acceptance Rate $\sim$ 25%)

93. Soumyasantha Laha, Savas Kaya, Avinash Kodi and David Matolak, "60 GHz Tunable LNA in 32 nm Double Gate MOSFET for a Wireless NoC Architecture," *14th Annual IEEE Wireless and Microwave Technology Conference*, Orlando, Florida, April 7-9, 2013.

94. Randy Morris, Avinash Kodi and Ahmed Louri, "Reconfiguration of 3D Photonic On-chip Interconnects for Maximizing Performance and Improving Fault Tolerance," *45th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-45)*, Vancouver, BC, Canada, Dec 1-5, 2012. (Acceptance Rate $\sim$ 17%)

95. Soumyasantha Laha, Savas Kaya, Avinash Kodi and David Matolak, "60 GHz OOK Transmitter in 32 nm DG FinFET," *IEEE International Conference on Wireless Information Technology & Systems*, Maui, Hawaii, Nov 11-16, 2012.

96. Randy Morris, Avinash Kodi and Ahmed Louri, "3D-NoC: 3D Reconfigurable Nanophotonic Interconnects for Multicores," *30th IEEE International Conference on Computer Design (ICCD)*, Montreal, Quebec, Canada, Sept 30Oct 2, 2012. (Acceptance Rate $\sim$ 27%)

97. Dominic DiTomaso, Travis Boraten, Avinash Kodi and Ahmed Louri, "Evaluation of Fault Tolerant Channel Buffers for Improving Reliability in NoCs," *55th International Midwest Symposium on Circuits & Systems (MWSCAS)*, Boise, Idaho, Aug 5-8, 2012.

98. Dominic DiTomaso, Soumyasanta Laha, Savas Kaya, David Matolak and Avinash Kodi, "Energy-Efficient Modulation for a Wireless Network-on-Chip Architecture," *55th International Midwest Symposium on Circuits & Systems (MWSCAS)*, Boise, Idaho, Aug 5-8, 2012.

99. Dominic DiTomaso, Soumyasanta Laha, Savas Kaya, David Matolak and Avinash Kodi, "Energy-Efficient Modulation for a Wireless Network-on-Chip Architecture," *10th IEEE International NEWCAS Conference*, Montreal, Canada, June 17-20, 2012.

100. Brian Neel, Randy Morris, Dominic DiTomaso and Avinash Kodi, Power-Efficient Photonic Network for Many-core Architectures, *Workshop on Lighter-than-Green Dependable Multicore Architectures*, held in conjunction with IEEE International Green Computing Conference (IGCC-3), June 5, 2012.

101. Yixuan Zhang, Randy Morris, Dominic DiTomaso and Avinash Kodi, "Energy-Efficient, Fault-Tolerant Unified Buffer and Bufferless Crossbar Architecture for NoCs," *Workshop on High-Performance Power-Aware Computing (HPPAC)*, held in conjuction with IPDPS'12, Shanghai, China, May 21-25, 2012.

102. Soumyasantha Laha, Savas Kaya, Avinash Kodi and David Matolak, "Double Gate MOSFET Based Efficient Wide Band Tunable Power Amplifiers," Accepted to appear in *13th Annual IEEE Wireless and Microwave Technology Conference*, Cocoa Beach, Florida, April 16-17, 2012.

103. Avinash Kodi, Randy Morris, Dominic DiTomaso, Ashwini Sarathy and Ahmed Louri, "Co-Design of Channel Buffers and Crossbar Organizations in NoCs Architectures," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, California, November 6-10, 2011. (Acceptance Rate $\sim$ 30%)

104. Dominic DiTomaso, Avinash Kodi, Savas Kaya and David Matolak, "iWISE: Inter-router Wireless Scalable Express Channels for Network-on-Chips (NoCs) Architecture," *19th Annual IEEE Symposium on High-Performance Interconnects (Hot Interconnects)*, Santa Clara, California, August 24-25, 2011. (Acceptance Rate $\sim$ 31%)

105. Randy Morris and Avinash Karanth Kodi, "Design of High-Speed Nanophotonic Architecture for Cache Coherent Multicores," *Optical Fiber Conference (OFC'11)*, OThQ6, Los Angeles, March 6-10, 2011.

106. Randy Morris and Avinash Kodi, "Scalable Nanophotonic Interconnect for Cache Coherent Multicores," in *Workshop on the Interaction between Nanophotonic Devices and Systems (WINDS)*, held in conjunction with MICRO-43, Atlanta, Georgia, Dec 5, 2010.

107. Randy Morris and Avinash Kodi "Design of On-Chip Networks using Microring-Resonator Based Nanophotonic Crossbar for Future Multicores ", *23rd Annual Meeting of the IEEE Photonics Society*, TB3, Denver Colorado, Nov 7-11, 2010.

108. Randy Morris and Avinash Kodi "Power-Efficient and High-Performance Multi-Level Hybrid Nanophotonic Interconnect for Multicores ", 4th *ACM/IEEE International Symposium on Network-on-Chips (NoCs'10)*, pp. 207-214, Grenoble, France, May 3-6, 2010. (**Best Paper Candidate**, Acceptance Rate $\sim$ 27%)

109. Jin Sun, Roman Lysecky, Karthik Shankar, Avinash Kodi, Ahmed Louri and Janet Wang, "Workload Capacity Considering NBTI Degradation in Multi-core Systems," *15th Asia and South Pacific Design Automation Conference (ASP-DAC'10)*,Taipei, Taiwan, Jan 18-21, 2010. (Acceptance Rate $\sim$ 34%)

110. Ravi Kiran Raghavendra, Avinash Kodi, Ahmed Louri and Janet Wang, "High-Speed Inter-Router Design for Network-on-Chip (NoC) Architectures", *Austin Conference on Integrated Systems and Circuits (ACISC'09)*, Austin, Texas, October 26-27, 2009.

111. Avinash Kodi and Randy W. Morris Jr., "Design of a Scalable Nanophotonic Interconnect for Future Multicores", *ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS'09)*, Princeton, New Jersey, October 19-20, 2009. (Acceptance Rate $\sim$ 23%)

112. Avinash Kodi, Randy W. Morris Jr., Ahmed Louri and Xiang Zhang, "On-Chip Photonic Interconnects for Scalable Multi-core Architectures", *3rd ACM/IEEE International Symposium on Network-on-Chip (NoCs'09)*, San Diego, California, May 10 - 13, 2009.

113. Avinash Kodi, Ahmed Louri and Janet Wang, "Energy-Efficient Router Buffers with Bypassing for Network-on-Chips (NoCs)," *10th International Symposium on Quality Electronic Design (ISQED'09)*, San Jose, California, pp. 826, March 16-18, 2009.

114. Sun Jin, Avinash Kodi, Ahmed Louri and Janet Wang, "NBTI Aware Workload Balancing in Multicore Systems," *10th International Symposium on Quality Electronic Design (ISQED'09)*, San Jose, California, pp. 833, March 16-18, 2009.

115. Avinash Kodi, Ashwini Sarathy, and Ahmed Louri, "Adaptive Inter-Router Links for Low-Power, Area-Efficient and Reliable Network-on-Chip (NoC) Architecture," *14th Asia and South Pacific Design Automation Conference (ASP-DAC)*,Yokohama, Japan, Jan 19-22, 2009. (**Best Paper Candidate**, Acceptance Rate $\sim$ 30%)

116. Avinash Kodi and Ahmed Louri, "Efficient Dynamic Bandwidth Re-allocation in Photonic Networks using SOI-based Microring Resonators," *Frontiers in Optics (FiO'08), OSA Annual Meeting*, FTuA2, Rochester, NY, October 19-23, 2008.

117. Avinash Kodi, Ashwini Sarathy, and Ahmed Louri, "iDEAL: Inter-router Dual-function Energy- and Area-Efficient Link design for Network-on-Chip (NoC) Architecture," Proceedings of the*35th International Symposium on Computer Architecture (ISCA'08)*, pp. 241-250, Beijing, China, June 21-25, 2008. (Acceptance Rate $\sim$ 14%)

118. Avinash Karanth Kodi, Ashwini Sarathy and Ahmed Louri, "Design of Energy-Efficient Adaptive Channel Buffers for Network-on-Chips Architecture", Proceedings of *ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS'07)*, pp. 47-56, Orlando, Florida, December 3-4, 2007. (Acceptance Rate $\sim$ 28%)

119. Avinash Karanth Kodi and Ahmed Louri, "Performance Adaptive Power-Aware Reconfigurable Optical Interconnects for High-Performance Computing (HPC) Systems", Proceedings of the *International Conference for High-Performance Computing, Networking, Storage and Analysis (SC'07)*, Reno, Nevada, November 10-16, 2007. (Acceptance Rate $\sim$ 21%)

120. Chander Kochar, Avinash Karanth Kodi and Ahmed Louri, "Implementation of Dynamic Bandwidth Re-allocation in Optical Interconnects using Microring Resonator," *Proceedings of 15th Annual IEEE Symposium on High-Performance Interconnects (Hot Interconnects 15)*, Stanford, California, pp. 54-64, August 22-24, 2007.

121. Avinash Karanth Kodi and Ahmed Louri, "Power-Aware Bandwidth Reconfigurable Optical Interconnects for High-Performance Computing (HPC) Systems", *Proceedings of 21st IEEE International Parallel and Distributed Processing Symposium, (IPDPS'07)*, Long Beach, California, March 26-30, 2007. (Acceptance Rate $\sim$ 26%)

122. Avinash Karanth Kodi and Ahmed Louri, "A New Technique for Dynamic Bandwidth Reallocation in Optically Interconnected High-Performance Computing Systems" in *14th Annual IEEE Symposium on High-Performance Interconnects (Hot Interconnects 14)*, Stanford University, California, August 23-25, 2006.

123. Avinash Karanth Kodi and Ahmed Louri,"Switchless Photonic Architecture for Parallel Computers" *Frontiers in Optics (FiO'05), 89th OSA Annual Meeting*, Tucson, Arizona, October 16-20, 2005.

124. Avinash Karanth Kodi and Ahmed Louri,"Scalable Optical Interconnection Network for Parallel and Distributed Computing" *Information Photonics (IP'05), Optical Society of America*, Charlotte, North Carolina, June 6-9, 2005.

125. Avinash Karanth Kodi and Ahmed Louri,"Design of a High-Speed Optical Interconnect for Scalable Shared Memory Multiprocessors" *12th Annual IEEE Symposium on High Performance Interconnects (Hot Interconnects 12)*, Stanford University, California, August 25-27, 2004.

126. Avinash Karanth Kodi and Ahmed Louri,"A Scalable Architecture for Distributed Shared Memory Multiprocessors using Optical Interconnects" *18th International Parallel and Distributed Processing Symposium (IPDPS'04)*, Santa Fe, New Mexico, April 26-30, 2004. (Acceptance Rate $\sim$ 39%)

127. Ahmed Louri and Avinash Karanth Kodi, "Parallel Optical Interconnection Network for SMPs," in *Frontiers in Optics (FiO'03), 87th OSA Annual Meeting*, Tucson, Arizona, October 5-9, 2003.

128. Ahmed Louri and Avinash Karanth Kodi, "Design of Large-scale Symmetric Multiprocessors (SMPs) using Parallel Optical Interconnects," in *Proceedings of the ACS/IEEE International Conference on Computer Systems and Applications, AICCSA '03*, p. 11, Tunis, Tunisia, July 14-18, 2003.

129. Avinash Karanth Kodi and Ahmed Louri, "Optical Interconnects for Large-Scale Symmetric Multiprocessor Networks," *In Proceedings of OSA, Optics in Computing 2002*, Tapei, Taiwan, April 2002.

130. Avinash Karanth Kodi and Ahmed Louri, "Y-junction Based addressing in Optical Symmetric Multiprocessor Neworks," *in Proceedings of International Annual Meeting of the Lasers and Electro-Optics Society, LEOS 2001*, La Jolla, San Diego, pp. 68-72, November, 11-15, 2001.

Patents

- Savas Kaya, Avinash Karanth, Talha Canan, "Ambipolar Field-Effect Device using Engineered Work-Function," United States Regular Patent 16/445,824 - December 19. 2019
- Avinash Karanth Kodi, Dominic DiTomaso and Ahmed Louri, "Directional Allocation of Communication Links Based on Data Traffic Loads," U.S. Patent No. 10,148,593 - December 4, 2018.

Professional Activities

- *Professional Membership*
  - IEEE Senior Member
  - ACM Member
- *Associate Editor/Topical Editor*
  - IEEE Transactions on Computers, 2019-.
- *Guest Editor*
  - Special Issue on Emerging Interconnect Technologies for Many-cores in IEEE Transactions on Emerging Topics in Computing (TETC), 2015-2016.
  - Special Issue on Network-on-Chips (NoCs) in Journal of Parallel and Distributed Computing, 2010-2011.
- *Organizing Committee*
  - *Special Issue Coordinator*, IEEE Transactions on Computers, 2019 onwards.
  - *Area Co-Chair*, EDA-1, System-on-Chip Design Methodology, Design Automation Conference (DAC), 2021.
  - *Area Vice-Chair*, Architecture track, 34th IEEE International Parallel and Distributed Processing Symposium (IPDPS), May 18-22, 2020.

  - *Finance Chair*, 25th IEEE Symposium on High-Performance Computer Architecture (HPCA), Washington DC, February 16-19 2019.
  - *Special Session*, 7th IEEE/ACM Symposium on Networks-on-Chips, May 2013.
  - *Workshop*, NSF Workshop on Emerging Technologies for Interconnects (WETI), Washington DC, February 2-3, 2012.
  - *Publicity Chair*, 13th IEEE Symposium on High-Performance Computer Architecture (HPCA), Phoenix, AZ February 13-16 2007.

- *Technical Program Committee Member*
  - 25th International Symposium on High-Performance Computer Architecture (HPCA-25), 2019.
  - 55th Design Automation Conference (DAC), 2018, 2019, 2020, 2021.
  - 12th IEEE International Conference on Networking, Architecture, and Storage (NAS), 2017.
  - ACM/IEEE International Symposium on Networks-on-Chip, 2016, 2017, 2018, 2019, 2020, 2021.
  - 3rd ACM International Conference on Nanoscale Computing and Communication, 2016, 2017.
  - IEEE International Symposium on Embedded Multicore/Manycore SoCs (MCSoCs), 2014, 2015, 2016, 2017, 2018, 2019.
  - (external) 45th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-45), 2012.
  - (external) 24th International Symposium on High-Performance Computer Architecture (HPCA-24), 2018.
  - Annual Symposium on High-Performance Interconnects (Hot Interconnects), 2010, 2016, 2017, 2019, 2020.

- *NSF Panel Member* - 2011, 2012, 2014, 2015, 2017, 2018, 2019, 2020.

- *External Peer Reviewer for Journals and Conferences*
  - IEEE Transactions on Computers
  - IEEE Transactions on Parallel and Distributed Systems
  - IEEE Transactions on Very Large Scale Integration (VLSI) Systems
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD)
  - IEEE Design and Test of Computers
  - IEEE Computer Architecture Letters
  - IEEE Journal on Emerging and Selected Topics in Circuits and Systems
  - ACM Transactions on Embedded Computing Systems (TECS)
  - OSA Optics Express
  - OSA Journal of Optical Society of America A (JOSA)
  - OSA Journal of Optical Communications and Networking
  - Journal of Parallel and Distributed Computing

  - OSA Applied Optics
  - Journal of System Architecture
  - Integration, The VLSI Journal
  - IEEE/ACM Symposium on Architectures for Networking and Communications Systems (ANCS'07)
  - IEEE Global Communications Conference (GlobeCom'08)
  - IEEE Asia Pacific Conference on Circuits and Systems (APCCAS'08)
  - IEEE International Symposium on High-Performance Computer Architecture (HPCA'09, HPCA'10, HPCA'11, HPCA'12)
  - IEEE Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS'14)
  - IEEE International Conference for High-Performance Computing, Networking, Storage and Analysis (SC'09)
  - IEEE International Symposium on Computer Architecture (ISCA'11, ISCA'12)
  - IEEE International Symposium on Microarchitecture (MICRO'11)
  - IEEE VLSI Design Conference (VLSI-D'15)

- *Graduate Students/Theses*

  - Current Graduate Students
    * Quintin Fettes (Ph.D.) co-advised with Razvan Bunescu - Expected Graduation in Dec 2021
    * Kyle Shifflet (Ph.D.) - Expected Graduation in December 2022
    * Siqin Li (Ph.D.) - Expected Graduation in May 2024
    * Saumya Chauhan (Ph.D.) - Expected Graduation in Dec 2025
    * Chris Evans (M.S.) - Expected Graduation in May 2023
    * Osoko Emmanuel (M.S.) - Expected Graduation in May 2023
  - *Dissertations*
    * Travis Boraten, "Hardware Security Threat and Mitigation Techniques for Network-on-Chips," Ph.D. Dissertation, Ohio University, Aug 2020.
    * Dominic DiTomaso, "Proactive and Reactive Fault Tolerant Network-on-Chips Architectures using Machine Learning," Ph.D. Dissertation, Ohio University, Aug 2015.
    * Randy W. Morris Jr., "Energy-Efficient and High-Performance Nanophotonic Interconnects for Shared Memory Multicores," Ph.D. Dissertation, Ohio University, June 2012.
  - *Theses*
    * Padmaja Bhamidipati, "RETUNES: Reliable and Energy-Efficient Network-on-Chip Architecture using Adaptive Routing and Approximate Communication," M.S. thesis, May 2019.
    * Mark Clark, "Dynamic Voltage and Frequency Scaling and Power-Gating of Network-on-Chips with Machine Learning," M.S. thesis, December 2018.
    * Scott VanWinkle, "Shared Heterogeneous Architecture with Reconfigurable Network-on-Chips," M.S. thesis, August 2017.

    - Juman Alshraiedeh, "Wear-out Leveling in Network-on-Chips (NoCs)," M.S. thesis, Ohio University, May 2017.
    - Ashif Sikdar, "Emerging Technologies in On-Chip and Off-Chip Interconnection Network," M.S. thesis, Ohio University, August 2016.
    - Matthew Kennedy, "Power-Efficient Nanophotonic Architectures for Intra- and Inter-Chip Communication," M.S. thesis, Ohio University, April 2016.
    - Travis Boraten, "Runtime Adaptive Scrubbing in Fault-Tolerant Network-on-Chips (NoC) Architectures," M.S. thesis, Ohio University, April 2014.
    - Brian Neel, "High-Performance Shared Memory Networking in Future Many-core Architectures Using Optical Interconnects," M.S. thesis, Ohio University, March 2014
    - Dominic DiTomaso, "Improving Energy-Efficiency of NoCs Using Emerging Wireless Technology and Router Optimizations," M.S. thesis, Ohio University, June 2012.
    - Yixuan Zhang, "High-Performance Crossbar Designs for Network-on-Chips (NoCs)," M.S. thesis, Ohio University, August 2010.
    - Hemsley Bien-aise, "Adaptive Shared Cache Migration Policy," M.S. thesis, Ohio University, June 2010.
    - Randy W. Morris Jr., "PROPEL: Power and Area-Efficient Nanophotonic Interconnect for Network-on-Chip," M.S. thesis, Ohio University, June 2009.

- *College/School Committees*
  - Stocker Faculty Enrichment Fund (SFEF) Committee 2010-2013
  - ABET Accreditation Committee Member 2008 - onwards
  - Quarter-to-Semester (Q2S) Computer Engineering (CpE) Committee Member 2008-2009
  - Quarter-to-Semester (Q2S) Electrical Engineering (EE) Committee Member 2008-2009
  - EECS Graduate Admission Committee (Electrical Engineering) 2009-2013
  - EECS Fund Allocation 2010-2013, 2014-2016
  - CpE/EE Computer Engineering Search Chair 2014, 2018
  - EE Lecturer Search Committee - 2015
  - Russ College Grant Coordinator Search Committee Member - 2014
  - Strategic Planning (LAB) 2010-
  - Research Committee 2014 -

- *Conference/Industry Presentations*
  - "High-Performance, Energy-Efficient, and Fault-Tolerant Network-on-Chip Design using Reinforcement Learning," *IEEE Design and Test in Europe (DATE)*, Florence, Italy, March 24-28, 2019.
  - "Designing Energy-Efficient Accelerators with Machine Learning for Advanced On-board Computing," *US Air Force Science and Technology 2030*, Indiana University, Bloomington, IN, May 10-11, 2018.
  - "Power-Efficient Kilo-Core Photonic-Wireless Hybrid NoCs," *32nd IEEE International Parallel and Distributed Processing (IPDPS-18)*, Vancouver, Canada, May 21-25, 2018.

– "Extending the Power-Efficiency and Performance of Photonic Interconnects for Heterogeneous Multicores with Machine Learning," *IEEE International Conference on High-Performance Computer Architecture (HPCA-24)*, Vienna, Austria, February 24-28, 2018.

– *[invited]* "Reconfigurable Photonic Network-on-Chip for Heterogeneous Multicores," *NSF CSR PI meeting 2017* in Orlando, FL, June 2, 2017.

– "Machine Learning Enabled Power-Aware Network-on-Chip Design," *IEEE/ACM Design Automation and Test in Europe (DATE-17)*, Lausanne, Switzerland, March 27-31, 2017.

– "Dynamic Error Mitigation in NoCs using Intelligent Prediction Techniques," *IEEE/ACM International Conference on Microarchitecture (MICRO-49)*, Taipei, Taiwan, October 15-19, 2016.

– "Secure Model Checkers for Network-on-Chip (NoC) Architectures," *26th ACM's Great Lakes Symposium on VLSI (GLSVLSI-16)*, Boston, MA, May 18-20, 2016.

– "Communication-Centric Many-Core Computing: Opportunities and Challenges," *University of Illinois, Chicago, ECE Department*, March 11, 2016.

– "Communication-Centric Many-Core Computing: Opportunities and Challenges," *University of North Carolina, Charlotte, ECE Department*, March 16, 2016.

– "Power and Performance Evaluation of Exascale Architecture using Photonics," *6th IEEE International Green and Sustainable Computing Conference (IGSC-15)*, Las Vegas, NV, Dec 14-16, 2015.

– "Cross-Chip: Low Power Processor-to-Memory Nanophotonic Interconnect Architecture," *Workshop on Energy-Efficient Networks of Computers (E2NC)* held in conjunction with (IGSC-15), Las Vegas, NV, Dec 14-16, 2015.

– *[invited]* "Communication-Centric Many-Core Computing: Opportunities and Challenges," *IEEE International Conference on Ubiquitous Wireless Broadband*, Montreal, October 4-7, 2015.

– "Design of Bandwidth Adaptive Nanophotonic Crossbars with Clockwise/Counter-Clockwise Optical Routing," *VLSI Design Conference*, Bangalore, India, January 5-7, 2015.

– *[invited]* "Scalable 3D Photonic Interconnects for Many-core Architectures," *PhoxTrot 1st Optical Interconnect in Data Centers Symposium*, Berlin, Germany, March 18-19, 2014.

– *[invited]* "Wireless Network-on-Chips: Potential and Challenges," *15th ACM/IEEE System Level Interconnect Prediction (SLIP)*, Austin, TX, June 2, 2013.

– "3D-NoC: 3D Reconfigurable Nanophotonic Interconnects for Multicores," *30th IEEE International Conference on Computer Design (ICCD)*, Montreal, Quebec, Canada, Sept 30Oct 2, 2012.

– "Co-Design of Channel Buffers and Crossbar Organizations in NoCs Architectures," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, California, November 6-10, 2011.

– "Design of High-Speed Nanophotonic Architecture for Cache Coherent Multicores," *Optical Fiber Conference (OFC'11)*, OThQ6, Los Angeles, March 6-10, 2011.

– "Scalable Nanophotonic Interconnect for Cache Coherent Multicores," in *Workshop on the Interaction between Nanophotonic Devices and Systems (WINDS)*, held in conjunction with MICRO-43, Atlanta, Georgia, Dec 5, 2010.

– "Switching Techniques and Architectures for Performance-Adaptive, Power-Aware, Hybrid Opto-Electronic Interconnects," ECCS-NSF Grantees Workshop, Honolulu, Hawaii, Nov 30-Dec 3, 2010.
– "Power-Efficient and High-Performance Multi-Level Hybrid Nanophotonic Interconnect for Multicores ", 4th *ACM/IEEE International Symposium on Network-on-Chips (NoCs'10)*, Grenoble, France, May 6, 2010.
– *[invited]* "PROPEL:Power and Area-Efficient Nanophotonic Interconnect for Future Multicores", Computer Science Department, *University of Pittsburgh*, November 5, 2009.
– "Energy-Efficient Router Buffers with Bypassing for Network-on-Chips (NoCs)," *10th International Symposium on Quality Electronic Design (ISQED'09)*, San Jose, California, March 16-18, 2009.
– "NBTI Aware Workload Balancing in Multicore Systems," *10th International Symposium on Quality Electronic Design (ISQED'09)*, San Jose, California, March 16-18, 2009.
– "Efficient Dynamic Bandwidth Re-allocation in Photonic Networks using SOI-based Microring Resonators," *Frontiers in Optics, OSA Annual Meeting*, Rochester, NY, October 19-23, 2008.
– "Performance Adaptive Power-Aware Reconfigurable Optical Interconnects for High- Performance Computing (HPC) Systems", *International Conference for High-Performance Computing, Networking, Storage and Analysis (SC'07)*, Reno, Nevada, November 10-16, 2007.
– "Board-to-Board Reconfigurable Optical Interconnects for High-Performance Computing Systems," *ECE Department, University of Rochester*, Rochester, New York, March 2007.
– "Board-to-Board Reconfigurable Optical Interconnects for High-Performance Computing Systems," *EECS Department, Ohio University*, Athens, Ohio April 2007.
– "Board-to-Board Reconfigurable Optical Interconnects for High-Performance Computing Systems," *ECE Department, University of Colorado*, Boulder, Colorado, April 2007.
– "Power-Aware Bandwidth Reconfigurable Optical Interconnects for High-Performance Computing (HPC) Systems", *21st IEEE International Parallel and Distributed Processing Symposium*, (IPDPS'07), Long Beach, California, March 26-30, 2007.
– "A New Technique for Dynamic Bandwidth Re-allocation in Optically Interconnected High-Performance Computing Systems" at the *14th Annual IEEE Symposium on High Performance Interconnects (Hot Interconnects)*, Stanford University, California, August 23, 2006.
– "Reconfigurable, All-Photonic Interconnect for Distributed parallel computing and storage area networks (SANs)", Progress Report for *Connection One*, ASU, Tempe, Arizona, 31 January, 2006.
– "Scalable Optical Interconnects for Parallel Computers" Progress Report at *Intel Corporation*, Santa Clara, California, Nov 1, 2005.
– "Switchless Photonic Architecture for Parallel Computers" at *Frontiers in Optics, 89th OSA Annual Meeting*, Tucson, Arizona, October 18, 2005.
– "RAPID: Reconfigurable, All-Photonic Interconnect for Distributed parallel computing ", Proposal presentation for *IBM/ECE Engineering Day*, Tucson, Arizona, 21 September, 2005.
– "Scalable Optical Interconnection Network for Parallel and Distributed Computing" at *Information Photonics, Optical Society of America*, Charlotte, North Carolina, June 9, 2005.

– "Optical Communication Networks for Large Scalable Parallel Computers" Poster Presentation at the *Connection One*, Semi-Annual Meeting, Tucson, Arizona, February 1, 2005.

– "Design of a High-Speed Optical Interconnect for Scalable Shared Memory Multiprocessors" at the *12th Annual IEEE Symposium on High Performance Interconnects (Hot Interconnects)*, Stanford University, California, August 26, 2004.

– "A Scalable Architecture for Distributed Shared Memory Multiprocessors using Optical Interconnects" at the *18th International Parallel and Distributed Processing Symposium (IPDPS'04)*, Santa Fe, New Mexico, April 27, 2004.