Workshop on Emerging Technologies for Interconnects

Final Report

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1. Introduction and Motivation

The International Technology Roadmap for Semiconductors (ITRS) projects that device scaling will continue well into the sub-nanometer regime, which in turn will provide opportunities to integrate an exponentially increasing number of transistors within a single chip [1]. For decades, computer architects used the additional transistors available from technology scaling to increase the performance of single core microprocessors in order to speed up sequential applications. Architectural features such as superscalar execution, speculation, deeper pipelines, and multi-level cache hierarchies were implemented in successive microprocessor generations in order to speed up existing sequential programs while requiring little attention from the application programmer.

In the early 2000s, improving performance using processor core architecture techniques became unsustainable from a power standpoint due to excessive heat and energy usage. The industry was forced to shift from implementing increasingly complex, power-hungry single cores to a multi-core approach where several (2-8) cores of modest complexity and frequency are implemented on a single die, and interconnected with a simple electrical bus or a set of point-to-point electrical links. As shown in Figure 1, clock frequency and single-thread performance increased from the 1970s until the shift to multi-core around the year 2004. At this point, frequencies and single-thread performance began to tail off and the number of cores began to dramatically increase.

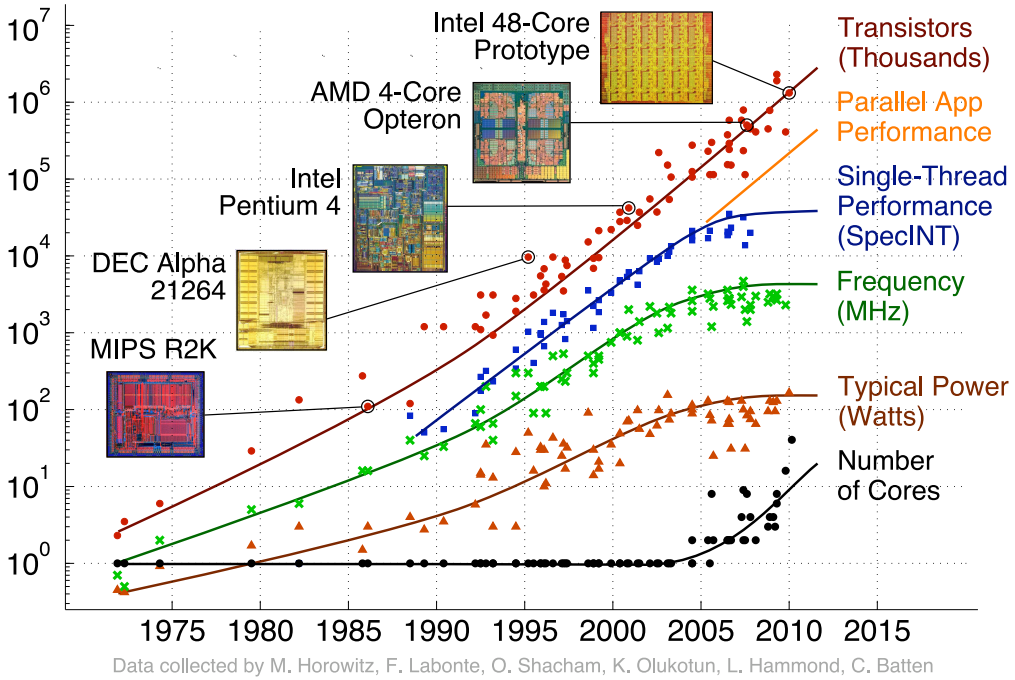

Figure 1: Processor trends from the 1970s up to the present day. Up until the early 2000s, computer architects used additional transistors available with Moore's Law scaling to increase the performance of a single core (thread). At this point, a *power wall* was reached, necessitating the move to multi-core computing. The number of cores on a die is currently increasing at an exponential rate, commensurate with Moore's Law. [Source: Christopher Batten]

The current exponential rate of increase in the number of cores has brought interconnects to the forefront of the challenges facing the computing industry. The

progression to hundreds to thousands of on-die cores—the many-core approach—and its associated on-chip and off-chip bandwidth requirements is leading to a *communications wall* where computer systems can no longer scale in performance, cost, energy efficiency, and programmability to support future applications due to discrepancies between computation and communication (both on-chip and chip-to-chip).

To further illustrate the interconnect challenges resulting from the move to many-core processing, consider the growing gap between the energy used for computation and for global communication (Figure 2). At 45nm, compute and communication energy were roughly equal. As technology scales to 7nm, the energy for computation is expected to decrease at a relative rate of 6X from the 45nm node, but by only a factor of 1.6X for global communication. This means that at 7nm the energy of global communication will be a factor of 3.75X higher than computation, which will make optimizing the power-performance efficiency of communications the overriding priority for computer architects.

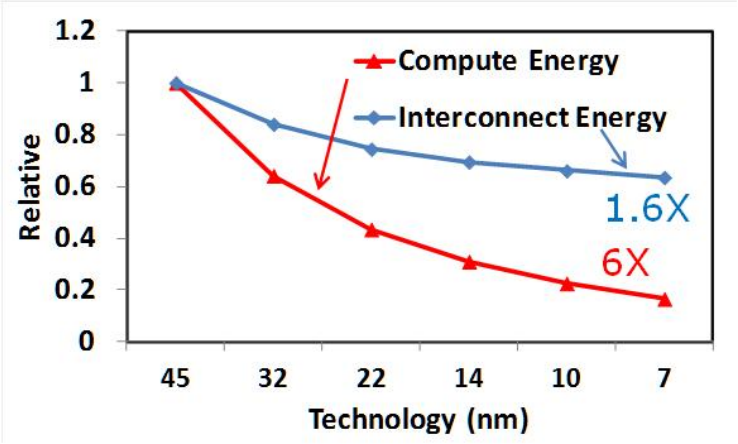

Figure 2: Comparison of the energy scaling trends for computation and global communication. At 45nm, the energy for each was roughly equal. At 7nm, the energy for global communication is projected to be 3.75X that used for computation. [Source: Shekhar Borkar]

For these reasons, the design and implementation of low latency, high bandwidth, and power efficient on-chip and chip-to-chip interconnection networks has become one of the most critical challenges to achieve the performance potential of future many-core systems. Industry and academia roadmaps suggest that alternatives to conventional metal interconnects will be needed to meet these demands [2-4]. While several promising alternatives have been identified, research in these areas has been largely limited in scope to specific areas of the computing stack, and little progress has been made across problem sub-domains. Thus, there is a dire need for holistic research efforts spanning the stack from physics to systems that produce prototypes and development tools of much greater sophistication than what is currently available in order to enable commercial adoption.

While interconnection networks (mostly macro-networks) have been a focus of study for several decades, research in chip-to-chip and on-chip networks (or Network-on-Chips (NoCs)) has surged in recent years, primarily due to the emergence of multicore architectures and the need for higher bandwidth chip-to-chip interfaces [5, 6]. NoCs and chip-to-chip networks have different cost-performance constraints than rack-level, board-to-board interconnects, that impact power consumption, area, and performance [7]. While metal on-chip networks can in theory provide sufficient bandwidth to support many-core

systems, the slow connectivity growth in packaging indicates an emerging scarcity of bandwidth to support multi-socket systems and inadequate memory bandwidth. In addition to these bandwidth density constraints, the various on-chip and chip-to-chip communication fabrics are fast consuming a major portion of the system power budget, leaving insufficient power headroom for cores, memory, and storage [8-10]. While electrical interconnects can perhaps attempt to address the energy-cost issue through extensive parallelism (just like in computation), the bandwidth density constraints are already tight enough to prevent any major strides in this direction. In other words, bandwidth constraints are forcing the links to operate faster and pushing them into the regime that is not energy-efficient. These major bottlenecks need to be urgently addressed to prevent future systems from stagnating in terms of performance. Due to the inability of electrical technology to overcome this dual energy-bandwidth constraint space, the research community must develop alternative interconnection technologies that have the potential to break these dependencies.

Recent research has shown that emerging technologies, such as nanophotonics, have the potential to reduce network power consumption by an order of magnitude at the same performance level as conventional metal interconnects [11, 12]. Nanophotonics has already demonstrated several advantages suitable for on-chip communication: distance-independent bit-rate, higher bandwidth density, higher performance-per-Watt, and many others. However, bringing optics into the chip presents a number of challenges such as device design and integration in fabrication flows as well as a multitude of packaging and reliability issues such as coupling signals, multiplexing multiple wavelengths, device losses, thermal stability, and laser design. [13-23]. Emerging technologies in general are largely untested in a full CMOS fabrication flow in on-chip communication (and to some degree chip-to-chip) and bring a host of challenges—from integration to packaging.

Another formidable barrier to the adoption of these technologies is that research advances have been piecemeal in nature and there is a lack of system-level demonstrations and mature cross-layer tools. The full exploitation of these alternative technologies requires holistic approaches whereby the devices, circuits, and system-level architecture (such as the cache coherent transfer mechanism and the memory controller design) are developed hand-in-hand. This requires the development of integrated tool flows that enable rapid iteration at each level of the stack, and cross-layer optimization, e.g., the ability to quickly characterize the impact of component tradeoffs on system-level metrics. Moreover, demonstrations of these new technologies have been extremely limited and largely confined to small, link-level demonstrations. Significant advances in fabrication, integration, packaging, testing, and validation must be made to enable more sophisticated system-level demonstrations of these technologies.

The Workshop on Emerging Technologies for Interconnects (WETI) was held February 2-3, 2012 in Arlington, Virginia in order to address these issues (http://weti.cs.ohiou.edu). Leaders from academia, industry, and government were brought together to define an agenda for the research and commercial adoption of emerging interconnect technologies that hold the promise of much greater power-performance efficiency than conventional metal interconnects. The remainder of this report presents the primary findings of the workshop and recommended follow-up actions.

2. Summary of Recommendations

To overcome the threat of the communications wall, the following actions are recommended:

1. There is no “magic bullet” at any one layer of the communication stack that will solve the communications bottleneck. Rather, a holistic research approach should be supported that spans the entire stack from devices to algorithms/applications.

2. Research is needed in NoC architectures for many-core systems, including work in hierarchical, heterogeneous systems employing mixed technologies, network switching approaches, and 3D integration.

3. The memory sub-system bottleneck must be addressed through improving the efficiency of memory data movement throughout the system, from the source (memory cells) to the destination (registers) and at every step along the way.

4. Interconnect network resilience is a significant pending concern, and requires efforts in understanding the defect and failure modes of the components of emerging interconnect technologies, and the development of cross-layer mitigation approaches that are cost effective and energy efficient.

5. Significant work is needed in developing new electrical solutions in the areas of novel circuits, new materials, devices/circuits/architecture co-design, packaging, and power delivery and management.

6. Nanophotonic networks hold great potential and research is required at multiple levels, including novel devices and circuits, network topologies, easing parallel system programmability, power management, and improving resiliency.

7. Significant work on crosscutting modeling tools should be supported, including cost-performance modeling tools and behavioral/cross-domain simulation tools that accelerate design and integration.

8. The creation of industry-relevant photonic technology should be supported by strengthening device and platform fabrication opportunities and forming a national center for nanophotonic platform fabrication.

9. Joint programs should be created with industry (perhaps with SRC mediation) to explore photonic integration opportunities in the definition of processes beyond 22 nm and special customizations at older generations.

3. Interconnect Challenges and Research Directions

Future many-core architectures with 100s to 1000s of cores present significant on-chip and chip-to-chip interconnect challenges, especially for emerging applications involving the processing of large data sets and requiring large-scale inter-processor communication. Examples of such applications include:

- *Big Data*: Data mining/analytics, Astrophysics, Genomics, medical imaging
- *Graph Processing*: Facebook, unstructured data, connectivity analysis
- *Streaming*: Video surveillance/processing, UAV, face recognition

The panel discussions and working group sessions identified a number of critical research challenges that must be addressed to prevent future many-core systems from becoming communication bound. One conclusion from the workshop is that the problem is so severe that no single "magic bullet" at one layer of the stack can alone provide a solution. Rather, a holistic approach that spans the entire stack from devices to algorithms/applications is necessary (Figure 3), including associated work in modeling methodologies and evaluation tools.

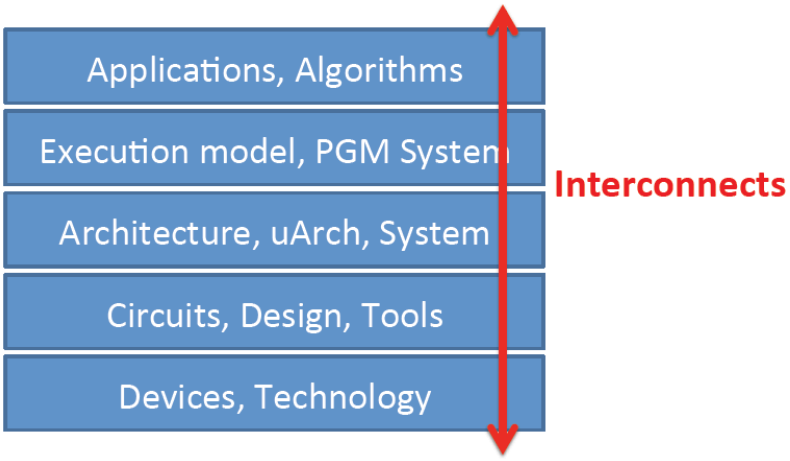

Figure 3: A holistic approach that spans the layers of the communications stack is needed to address the pending communications wall.

The workshop focused on four major research areas: system architecture; electronics microarchitecture, circuits, and devices; nanophotonic microarchitecture, circuits, and devices; and crosscutting tools. Each of these areas is discussed in the remainder of this report.

3.1 System Architecture

A significant research effort is needed at the system architecture level, irrespective of the underlying technology, e.g., electronics or nanophotonics, particularly in the following areas.

3.1.1 Network-on-Chip (NoC) architecture

The energy expended for data movement will have a critical impact on achieved performance of a future many-core system. Every nano-joule of energy used to move data up and down the hierarchy, as well as to synchronize across and move data between the cores, takes away from the limited power budget, and reduces that available for computation. In this context, efficient networks, including those on chip (NoC), become critical to ensuring that future systems do not stagnate in terms of performance.

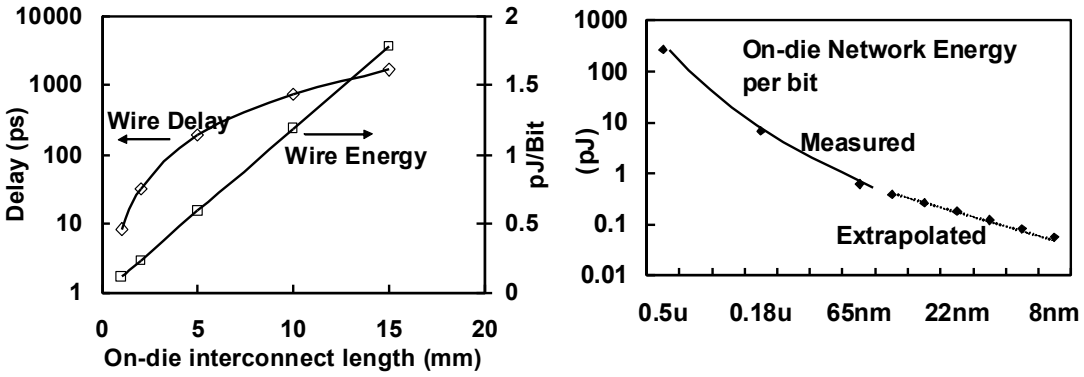

Figure 4: On-die interconnect (a) delay and energy to move one bit across a processor die at 45nm, and (b) energy to move one bit one hop in a NoC with technology scaling. [Source: Shekhar Borkar]

Figure 4 shows the typical wire delay and energy required to move one bit of data on the processor die, and the energy consumed in moving a bit across a hop in a NoC. The data is derived from measurements on historic networks, and extrapolating to the future with scaling assumptions. Considering a future 3 Tera-Ops processor, with only 10% of the operands moving over the network traversing 10 hops on average, then at the rate of 0.06 pJ/bit the network power alone would be 35 Watts, or more than half the power budget of the processor. Note that this prediction is very optimistic, since most likely large diameter networks (e.g., mesh) will not be favorable due to latency for large many-core systems; hence networks with more global links (like Clos or fat-trees) may be used, where the energy scales even more slowly than in Figure 4.

In the future, data movement over these networks will have to be limited to conserve energy, and due to large local storage, data bandwidth demand on the network can be reduced. In light of these findings, one possible approach to on-die network architectures is hybrid packet/circuit switching, where wide circuits are built using a narrow packet switched network, and a large amount of data is transferred over a wide established circuit. These circuit switched topologies could use circuit technologies such low swing differential signaling to further reduce the energy of data movement.

Small cores in close proximity can be interconnected into clusters with traditional buses, which are energy efficient for data movement over short distances. The clusters are connected using wide (high bandwidth) low-swing (low energy) buses, or with packet or circuit switched networks depending on the distance. Hence, the NoC could be both hierarchical and heterogeneous, a departure from the traditional parallel machine approach.

Additional levels of hierarchy, organized differently than the lower levels, may be required in larger-scale many-core systems. While the physical interconnect design may be hierarchical, a key objective is to achieve as much as possible a flat view of memory from the programmer's perspective. Radical departures from conventional designs will be needed to overcome the challenges posed by the electrical NoC fabric design.

Power management in the network is challenging, since any power management technique, such as clock gating or sleep-states, incurs wake up latency, which impacts system performance. On the one hand, smaller cores give higher throughput performance in the same power envelope, but on the other hand, this increases the number of network nodes, increasing the network power. Moreover, with the number of cores increasing from hundreds to thousands, runtime power management in proportion to the application workload will become critical. Runtime power management may dynamically adapt the network to match the application behavior. In addition to power management techniques, new network implementation approaches should be considered, possibly with emerging technologies, such as through-silicon-via (TSV) based 3D integration.

One potential solution is to design a dedicated NoC die fabricated on process technologies optimized for the NoC, and 3D integrated with TSVs that is separate from the die holding the processor cores and on-chip memory. For example, the NoC chip could have a different metal system, and may have different transistors and passives optimized for the NoC application The resulting system incorporates two different technologies, one optimized for high performance processor cores, and the other for the NoC. The result is that each technology does not detract from the other due to its specific optimization requirements, without increasing the system cost. These types of systems require very tight-pitch TSV technology and improvements in 3D stacking.

3.1.2 Memory sub-system architecture

In a modern server, the memory system accounts for roughly one-third of the total power dissipation. More than half the execution time in many large-dataset workloads can also be attributed to memory accesses. It is expected that next-generation processor chips will employ computational cores that are more energy-efficient (by employing simpler pipelines, with near-threshold computing, etc.). Correspondingly, there needs to be significant innovation on the memory side. If this is not done, the high cost of memory access will impede our progress towards increasingly power-efficient servers and consumer systems.

The memory system presents several important challenges that must be tackled in the coming decade:
(1) *Power*: the high cost of data storage and data movement must be reduced.
(2) *Bandwidth*: the stagnation in processor pin count will require new breakthroughs to feed processor chips with a growing volume of data.
(3) *Latency*: the high latency for memory access has several components, some of which have the potential to be alleviated or tolerated.
(4) *Capacity*: a large number of memory modules must be connected to each processor chip without negatively impacting other metrics (latency, power, bandwidth).

(5) *Reliability*: the memory system will be a growing source of errors that will require efficient fault tolerance methods.

All of the above challenges have their roots in the fact that every memory access requires movement of several thousand bits over relatively long distances at relatively high speeds. A memory access activates tens of thousands of DRAM cells that are brought to sense amplifiers (row buffers) over global wires, hundreds of bits are then sent over global wires to the DRAM chip's center stripe, these hundreds of bits are then sent over off-chip links to buffer chips and then finally to the processor chip. This has been the norm for several decades because of memory standards and programming models that evolve slowly, and because the DRAM industry has prioritized density and bandwidth over other metrics. It is evident that the memory system architecture must be overhauled to meet the low energy per operation targets of future machines. These new architectures must support a reduction in data movement and efficient interconnects to handle data movement that is unavoidable. While there are several avenues to achieve these goals (many that are yet to be discovered), we list a few avenues here as concrete realizable goals.

Data movement can be reduced by moving some of the computation closer to the memory. Such "processing-near-memory" can be best realized with emerging 3D technology that can place a processor chip and memory chips in a single 3D package, connected with efficient TSVs. Programming models must also be developed to facilitate such processing-near-memory architectures. Moreover, this use of 3D technology must be reconciled with the use of 3D for on-chip networks as discussed in the previous section. Both goals are important for performance and power efficiency, but the constraints of large scale 3D stacking must be addressed.

Data movement can also be reduced by addressing the amount of over-fetch within memory chips, and by intelligently placing data pages within a networked memory system such that frequently accessed data is reachable with a minimum number of hops. The emergence of new memory cells (PCM, STT-RAM, etc.) implies that the memory hierarchy will grow deeper, requiring intelligent caching strategies to limit data movement between different levels of the hierarchy. Reduction in data movement can also be achieved by reorganizing memory controllers so that some functions are performed on the processor chips and some on the memory chips; this is especially true for emerging PCM chips that require more "maintenance" (wear-leveling, hard error tolerance, drift detection, etc.).

The efficiency of data movement can be improved by designing better on-chip links, off-chip links, and routing elements. Again, the TSVs and superior logic circuits made possible by 3D packaging represent a huge opportunity in this regard. Photonic links are also a major opportunity, especially since they have the potential to overcome the memory bandwidth wall. The buffer chips that serve as routing elements in a large networked memory system have received little attention from the research community and offer much room for improvement as well.

3.1.3 System-level resilience

Late CMOS era designs will encounter the problem of dealing with increasingly unreliable devices and interconnect components. The successful transition from metal

interconnects to non-traditional materials will be highly dependent on the development of models and tools for the analysis of new generation fault (or defect) models. Classic fault-tolerant interconnection network approaches will need to be revisited and re-adapted to fit the needs that are exposed by these newer fault models. Even with regard to metal interconnects and C4 pads, late CMOS era scaling will require significantly larger attention to failure mechanisms like electromigration and stress migration. Joule heating effects can no longer be ignored in that regime, and will only exacerbate the problem of power density and thermals. Many-core architectures in this regime will have to live with the notion of less than perfect yield when it comes to on-chip network functionality. Also, a subset of the network will face the prospect of early "death" due to the lower-cost chip burn-in methods that are likely to be adopted during this design era.

The permanent failure models of most concern in the late CMOS era regime are:

(1) Time-dependent dielectric breakdown (TDDM);
(2) Negative (or Positive) bias temperature instability (BTI) and Hot Carrier Injection (HCI);
(3) On-chip voltage regulation module failure; and
(4) Electromigration-induced shorts and opens within the core.

The transient and intermittent failure models of relevance are:

(1) Single and multi-event upsets induced by high energy cosmic particles or package-sourced alpha particles, particularly problematic for storage structure such as buffers;
(2) Thermal hot spot induced circuit critical path delay faults;
(3) Inductive noise transients on the supply voltage line, causing potential violation of critical path delay constraints; and
(4) BTI-induced intermittent circuit timing failures, preceding the onset of permanent failures across all operational data input.

Many of these failure mechanisms are becoming more severe with technology scaling due to the double-edged sword of growing individual component failure rates and an exponential increase in integrated components. With the growth in NoC and processor-memory communication components comes a critical need to create architecture-level resilience techniques that address growing network component failure rates in the most energy-efficient manner possible.

Alternatives to electrical interconnect, such as nanophotonics, hold great promise but as relatively new technologies, their failure mechanisms are far less understood. A significant research effort in nanophotonics reliability is required along two fronts:

(1) Developing a deep understanding of the underlying failure mechanisms of nanophotonic devices such as lasers, rings, and receivers (which ties to physical design models, Section 3.4.2), including intrinsic manufacturing defects when manufactured at scale; and
(2) Exploring the combination of measures at the device, circuit, microarchitecture, and system architecture levels that could most cost-effectively address transient and permanent failures and defects.

Many-core processor architectures will need built-in resilience factored into the design through interconnect-level redundancies and associated fault-tolerant messaging protocols.

Wear-leveling techniques incorporated via wear-out and variability-aware task scheduling need to be incorporated into cross-stack resilience management architectures.

3.2 Electronics Microarchitecture, Circuits, and Devices

The workshop explored architecture, circuits, and devices for emerging electronics interconnect technologies. The key research directions highlighted by the electrical interconnect working group are as follows.

3.2.1 Novel interconnect circuits

Today's systems employ a variety of circuit architectures for communicating within a chip, across a package or socket, across a board, and between boards. However, the costs of these circuits, measured both in energy and in area, project to overwhelm our silicon resources as we increase system scale and capability. For communication on a chip, wires are plentiful but RC-limited, and challenge designers to best arrange them in networks with optimal radix, connectivity, and radius. Data moving between chips must confront the limits of solder, which restricts the number of available IO channels and drives designers to push the frequency limits of serializer/deserializer (SerDes) links. And for long distance data movement, the adversarial environment presented by traditional (low-cost) cables and traces forces designers into increasingly complex channel equalization technologies.

Therefore, we need to develop a suite of new interconnect circuit architectures with disruptive improvements not only in performance (bandwidth, latency, and reliability) but also in cost and overhead (area, energy, manufacturability, complexity, and testability). Such solutions must address the diverse set of constraints both on and between chips, and should accommodate likely changes in device technologies, materials, system architectures, and heterogeneity. They must also account for the myriad of new challenges arising from device scaling and how these impact different circuit elements differently. Finally, interconnect solutions need to both support and enable system architectures that employ increasing adaptability or reconfigurability. Dynamic redeployment and migration of both compute and data across future large-scale systems will demand not only highly efficient and flexible interconnect fabrics, but also multiple interconnect levels of "metadata" for system reconfiguration.

New circuit architectures can include new link transceivers (such as those for optics), inductive or capacitive coupling, RF/wireless, terahertz signaling, or transmission lines. They can also include advances in circuit styles such as mixed-signal/analog IO with low-swing signaling. Or they can integrate several heterogeneous technologies. Technologies that trade off significant gains in one dimension for substantial degradation in another should be carefully considered, as they may have difficulty in supplanting conventional interconnect technologies. A very important aspect in the circuit design of these emerging transceivers is the ability to power-manage the links quickly (i.e., rapid on/off regime) to support advanced power-management strategies at the network and system level. Currently, this has been a big problem in electrical transceivers due to the need to both settle bias nodes in various analog/mixed-signal circuits as well as perform synchronization. The development of circuit design and clocking architectures that support these instant-on operating regimes will help significantly in improving the overall system efficiency.

3.2.2 Novel materials for density, performance, and reliability

Material advances can play a strong role in improving the performance and cost profile of interconnects. The dimensions of on-chip metal lines typically push them into RC-limited behavior, so material advances that reduce material resistivity and dielectric permittivity are welcome. At the same time, new materials must address concerns about long-term metal reliability through electromigration and void propagation, dielectric material strength during assembly and packaging, and thermal conductivity in 3D-stacked systems. We note that material advances include not only the introduction of new materials (such as the historical examples of low-k metal dielectrics, high-k gate dielectrics, and Ge strain) but also the ability to post-process existing materials. Such technologies might include fluidic channels in silicon or oxide, selective etch for reduction of thermal conductivity and thermal mass, tight-pitch through-Si vias, and so on. Also, at the chip, package, and socket level, materials have a strong impact on interconnects. Off-chip IO pitch—today, set by solder deposition and pick-place assembly—can be improved through advancements in both package materials and surface features to improve assembly alignment. Finally, materials used to construct IO channels have a strong impact on the energy efficiency of link transceivers, by affecting overall channel loss and dispersion. In such dense package routing environments, the fundamental density limits due to capacitive and magnetic cross-talk should be investigated.

3.2.3 Interconnect devices/circuits/architecture co-design

The design of next-generation interconnects must consider cross-layer tradeoffs, involving issues of manufacturing, devices, circuits, architecture, and software concurrently. Optimization in a single domain may not deliver as much impact as joint optimizations between two or three disciplines. For example, the requirement for fast-wakeup of on/off links requires specifications of link utilization patterns and scheduling from architects. Another co-design example is the design of temperature-stable ring resonator silicon photonics, where collaboration is required from material scientists (who understand thermal expansion), CMOS designers (who can build closed-loop temperature sensing/actuation feedback), computer architects (who can estimate the spatial/temporal temperature changes based on workload), and others. While the above are just a small subset of examples, it is vital that future interconnect designers not only innovate within their own specialty but can collaborate together to achieve a larger system-level benefit.

3.2.4 Packaging of heterogeneous technologies

Recent advances in heterogeneous integration make it possible to completely re-imagine the construction of large-scale systems. The development of 3D technologies and the ability to stack or package together die/wafers fabricated in diverse processes opens up not only a new spatial dimension, but also a new heterogeneous toolbox of circuits and devices from CMOS, MEMS, and photonics that can now be utilized within the same dense system. While non-idealities imposed by through wafer vias and thermal management still arise, heterogeneous integration offers intriguing new paradigms and research questions. A heterogeneous package, co-designed with novel interconnect technologies, includes not only the ability to build “up” with vertical stacks of chips, but also the ability to build “out” with different stacks connected through an efficient, high-bandwidth interconnect fabric.

For such systems, a key question hinges on “optimal” partitioning: how do we separate tasks—from compute, storage, and communication—between technologies and layers? As part of this question, designers must understand when integration within a single layer is more or less advantageous than segregating across different layers and co-packaging or stacking them together. In such systems, the ability to tailor system assemblies for specific applications offers the possibility of mixing and matching technology combinations to achieve the highest advantage for a given workload. Of course, understanding how these technologies affect system testability, yield, and manufacturability becomes a critical requirement as well.

3.2.5 Power delivery and management

Power is one of the most critical constraints for future computing systems, including on-chip and processor-memory networks. This system driver concerns not only power consumption and energy-efficiency, but on all aspects necessary to support its usage, such as: high efficiency power delivery and distribution; generation, regulation, and utilization of multiple supplies for large heterogeneous systems with workloads that vary both across space and time; thermal effects on performance and reliability; circuits and VLSI systems that exploit new technologies and innovations in power consumption and energy-efficiency; on/off-chip voltage regulators that achieve high-efficiency and high-bandwidth; and architectures that exploit utilization patterns to schedule and/or predict which blocks require more or less power. Ideas that simultaneously address multiple issues, with closed-loop feedback between different layers to optimize energy-efficiency, will be especially beneficial for future interconnect systems.

3.3 Nanophotonics Microarchitecture, Circuits, and Devices

The workshop explored architecture, circuits, and devices for emerging nanophotonics interconnect technologies. The key research challenges highlighted by the nanophotonics interconnect working group are as follows.

3.3.1 Novel nanophotonic devices/circuits

Based on the current bottlenecks of the electrical interconnects and projections of future process capabilities and compute requirements, the workshop participants identified the most promising directions for system design with nanophotonic interconnects. Further research and implementation effort is required in these areas:

- New scalable photonic devices for flexible resource utilization and optimization of network/system (e.g., switched on/off for efficient bandwidth utilization)
- On-chip/off-chip data interface between compute/memory and photonic network
  - Address the discrepancy between on-chip low speed clocking and the need for high off-chip bandwidth density
  - Develop control mechanisms for dense WDM, dense integration, sources and detectors, driven by energy-efficiency of the overall system

For these areas, the system design considerations include the following:

- Creating a flat interface between nodes using low latency and high bandwidth photonics, favoring simplicity and less hierarchy, thereby easing programmability
- Revisiting network/CPU functionality with low latency networks and cross-layer optimization
- Quantifying the benefits in programmability and performance of moving to coherency islands of 100 to 1000 cores through optical coherency traffic among sockets

3.3.2 System architectures leveraging optical network technology

A key research question is how architects can best leverage the latency/bandwidth/energy advantages of nanophotonics interconnects in order to improve performance and ease software development. The following areas should be explored.

3.3.2.1 Nanophotonic network topologies

The different properties of nanophotonic devices—including area, latency, bandwidth, energy, and failure mechanisms—means that previous network topology findings for electrical interconnects do not directly apply to nanophotonic networks. A number of topology studies have been performed for nanophotonic networks, but these have used limited applications and rough modeling methodologies and did not take important considerations—including system reliability and dynamic power management capabilities—into account.

A number of possible topologies (hierarchical, heterogeneous, flat, etc.) can be implemented using nanophotonics, and each of these brings a number of complex design trade-offs, including the switching complexity, component complexity, and energy costs. Hierarchical topologies could segregate the network into multiple layers for local and global communication, thereby enabling more scalable architectures. The network design for one layer can be replicated in multiple layers in order to build large-scale networks using nanophotonics. The risk in such an approach is that the latency could become problematic for particular types of applications. Work is needed in exploring nanophotonic network topologies that meet both bandwidth and latency requirements for a variety of applications.

Nanophotonics can be combined with other technologies in addition to electronics, such as RF/wireless circuits. Heterogeneous architectures that combine the benefits of multiple technologies could yield better performance-per-Watt than homogeneous approaches. RF/wireless interconnects can provide other advantages for long-range communication as these interconnects are CMOS compatible, waveguide-free (particularly wireless) and energy-efficient. Inter-chip core-DRAM communication could benefit from RF/wireless designs. Moreover, 3D stacking can bond multiple discrete dies (cores, caches and interconnect). Significant research effort is needed in architecting and evaluating such heterogeneous interconnect systems that combine multiple emerging technologies.

3.3.2.2 Easing the programmability of many-core machines

Today's electrically connected many-core hardware platforms prevent severe challenges to parallel programmers due in part to their many levels of hierarchy. Nanophotonics has the potential to help break through the parallel programming conundrum presented by many-core machines. One example where nanophotonics can ease parallel programming is through their ability to broadcast via signal splitting. Such natural broadcast can be useful in shared memory programming models that implement coherent protocols (snoopy or directory cache coherence).

Research is needed along two fronts:

(1) Identifying applications that can be parallelized efficiently with today's parallel programming techniques, and determine how they can be modified to take advantage of the increased efficiency of nanophotonic networks; and
(2) Understanding and quantifying the ways that nanophotonic interconnects can create systems that make parallel programming easier than on electrical networks (e.g., flatter machines and more efficient broadcast and coherency protocols).

3.3.2.3 Application of nanophotonics to consumer-class systems

Research in nanophotonic interconnects thus far has focused primarily on high-performance computing. While the focus is slowly shifting towards embedded systems, the emphasis today is relatively high-performance computing, not ultra-low-energy, portable applications (e.g., smartphones and tablets). The applications in these areas have different characteristics than those at the high end, and studies are needed with appropriate applications to understand how nanophotonic interconnects can help improve the energy consumption of consumer systems in addition to datacenter servers.

Key questions are related to the efficient utilization of the network components, including the laser, given network usage variation, including low utilization of the network for applications with modest network requirements. A significant challenge is the temperature sensitivity of nanophotonic devices, which requires thermal tuning. Techniques similar to low-power electrical circuit/system designs (power/thermal management, gating, power throttling, sharing) need to be investigated in nanophotonic networks together with the evaluating the most suitable network topologies to support such power management techniques.

3.3.2.4 Resilient nanophotonic networks

In comparison to electrical interconnects, relatively little work has been performed to understand the intrinsic manufacturing defects and failure mechanisms of nanophotonic devices such as lasers, rings, and receivers. Work in making nanophotonic networks that are high performance and energy efficient will be for naught if their yields are too low and their resilience after deployment cannot be assured.

Since chip-level nanophotonics is still an emerging technology, the exact form and frequency of link errors in a real system is less understood than the individual sources of errors—which include cross-talk between wavelengths in the same waveguide, thermal drift, and the stochastic nature of photodetectors—and the effects of process and temperature variations. Significant research effort is needed to understand defect and failure modes for nanophotonic devices manufactured at large scale.

Once these mechanisms are well understood, then a holistic multi-layer approach involving devices to systems, similar to that used in electrical systems, can be developed to address defects and in-situ failures. Interdisciplinary teams of architects, information coding and communication system theorists, circuit designers, and nanophotonics technologists are needed to develop solutions that meet defect and failure rate requirements in the most cost-effective manner.

3.3.3 Seizing the opportunity to create industry-relevant photonic technology

The current state of the photonic technology development in both academia and industry does not offer a clear path to the realization of photonic technology's potential. Currently, the technologies are either created in academic "CMOS compatible" environments [24-26], that have a hard time transitioning into state-of-the-art foundries, or they are locked to the older process nodes in CMOS foundries without the ability to follow the advanced process nodes and material systems and fabrication constraints associated with modern processes [17, 27-31].

The effort to overcome these challenges is already underway through research on how existing advanced processes [32-34] can be utilized for nanophotonic integration [18, 35-37]. However, the biggest benefits come from close interaction with CMOS foundries and, unfortunately, these activities have mostly started outside the U.S. (EpixFab in Europe – IMEC, LETI, [27], and various efforts in Asia: Singapore – IME, and Japan).

In order for the U.S. to regain the lead position in this important area for the future of manufacturing and computer-systems scaling, the workshop participants identified three main directions of investment and research:

- *Joint programs with industry to explore photonic integration opportunities in the definition of processes beyond 22 nm and special customizations at older generations*: Monolithic integration is key to lowering the production costs as well as energy consumption, while increasing the bandwidth density of communication and providing seamless on-chip and off-chip communication. Even though previous work has demonstrated that it is possible to introduce the photonic components into the front-end of the advanced CMOS process without any process changes, the real opportunity for high-performance photonics lies in looking ahead at nodes that are currently being defined and working with industry to explore the integration opportunities and constraints of these new process generations. Small changes to the process could lead to huge improvements in overall system performance due to nanophotonic interconnect and increase the value of the technology and return on investment. On the other hand, special customizations of older generation processes

can also help increase the lifetime of the technology and return on investment, while serving a number of applications.

- *Broad exploration of photonics in bulk CMOS*: The majority of the silicon-photonic technologies developed today are locked into the SOI platform, which has a minor part of the overall semiconductor volume and fabrication throughput. The key step to truly making photonics mainstream and impacting the majority of compute systems lies in bringing the photonics into bulk CMOS processes. The challenges and opportunities lie in a combination of constraints that emerge from further process scaling, such as thinner films and lower supply voltages as critical design constraints, as well as new material systems being introduced as opportunities in photonic device design technology:
    - Leveraging new materials for photonics including poly-silicon, SiN and novel complex oxides
    - Devices for ultra-low voltage swings as the node scales and ultra-low energy devices at high voltage
    - Detectors and sources and their integration
    - Leveraging nano-patterning capabilities of advanced process nodes to overcome the thin-film challenges

- *Advanced research on packaging technology via fundamental device and integration*: In order to successfully establish these activities, a broad coordination effort needs to be established around a state-of-the-art foundry hub, where both the academic community and industry can aggregate to jointly explore these integration and process development opportunities without contaminating their own production lines. One such opportunity is OpSiS, led by Prof. Hochberg, [38, 39], as well as the CNSE Fabrication Facility in Albany, NY, which already serves as the derivatives development foundry and a center for many semiconductor alliances. A broad NSF-SRC-DOD-DOE initiative could help establish this center as a world-leading technology hub for nanophotonic integration and process development. The CNSE has already started the photonic process development activities as a part of a DARPA DAHI program and several other industry initiatives, but more focused funding and goal structure are needed to create a productive photonic technology integration hub.

In this context, in addition to technology development, the research hub would provide the infrastructure for device and system prototypes without which it is difficult to continue to refine the system design and programming models and establish the true benefits of the nanophotonic technology at the system level. This prototyping service would enable:

- Comprehensive tool chain framework
- Characterization folded back into framework
- Packaging (with SRC participation)
- Early MOSIS-like fabrication service

The goal is moving up the stack to architecture and system design and simulation of meaningful applications to enable architecture research and reduce risk of adoption.

3.4 Crosscutting Tools

A crosscutting tools working group focused on one emerging technology, nanophotonics, although the ideas and recommendations can by and large be applied to other emerging technologies. Two major modeling tool challenges were identified. The first challenge lies in the inadequacy of today's system modeling stack to tightly connect the layers of hierarchy and expose to the system level the dependencies from lower level parameters (such as, for example, the lowest-level technology parameters) and perform fast design space explorations and sensitivity analysis. The second challenge is the lack of physical modeling and design tools that would enable reliable and efficient design of nanophotonic devices integrated into circuits and systems, where links and whole networks of photonic devices can be simulated and verified in a standard chip-design electronic design automation environment.

3.4.1 Crosscutting system modeling

Today, while there are extensive, rigorous models of individual photonic devices, system-level tools that integrate an entire die of photonics devices with supporting CMOS electronics and processor cores are still in their infancy. It is critical not only to integrate various photonic components and devices into a photonic lightwave circuit, but also to be able to model the interactions between CMOS and photonics, so that tradeoffs can be rigorously analyzed and optimal design decisions can be taken. There is thus a strong need for *automated, integrated, iterative design space exploration methodologies* that enable rapid evaluation of performance, energy, reliability and cost for emerging interconnect technologies. Achieving this goal requires three inter-related research activities.

3.4.1.1 Crosscutting modeling and automated optimization

The exceptional progress in the production of electronic systems over the last four decades would not have been possible without a parallel progress in the development of computer-aided design (CAD) methodologies and tools. The electronic design automation (EDA) academic and industrial community has provided a variety of automatic methods and solutions for design optimization and validation that accompany engineers throughout all stages of the design process while spanning from the device level through the circuit, micro-architecture and system levels.

Similarly, the development of an integrated suite of design methodologies and tools will be critical for the success of emerging technologies for interconnects. New models are necessary to capture at different levels of abstraction the properties of these technologies, which are often fundamentally different from traditional electronic devices and in many cases are still evolving. Fundamental research questions must be answered to develop new tools that can automatically combine heterogeneous components from emerging technologies, such as nanophotonics, with more traditional electronic technologies. Also, these tools have to be calibrated against chip prototypes as they become available, and readily updated to reflect new process and device innovations.

For instance, similar to electronic isolation, nanophotonic components and devices that have to be integrated into circuits need to be free of electromagnetic interference of nearby elements (near field interactions) to assure the desired performance on an integrated system level. CAD tools for the optimization and validation of this integration process are critical. On the other hand, more abstract models are necessary at the system level to support automatic design-space exploration and optimization of networks and micro-architectures.

3.4.1.2 Efficient simulation of large-scale heterogeneous systems

Simulators are a particularly important class of CAD tools and the quest for high-speed simulation of computing systems has incessantly continued over the years. The new class of emerging technologies for interconnects will enable the design of extremely large scale systems that combine many heterogeneous components, which in turn will require the development of a completely new class of very fast simulators. Here, a key research question is how to effectively leverage the freedom from backward compatibility issues to develop simulators that can effectively exploit the large degree of parallelism provided by the next generation of many-core platforms.

Another important question is how to support the simulation of these large-scale heterogeneous systems with complex application scenarios, which requires addressing the current lack of driving applications that are bandwidth intensive and latency sensitive, and push the limits of many-core chips. For example, currently available SPLASH and PARSEC benchmarks heavily underutilize even existing electrical networks and do not represent the applications that could potentially leverage large bandwidth-density of the nanophotonic interconnects.

3.4.1.3 Ecosystem for interdisciplinary research and education

Research in emerging technologies for interconnects such as nanophotonics inherently involves multiple disciplines. This mandates a need for an *ecosystem that enables interdisciplinary communication across abstraction layers*. Currently, due to the infancy of the field, many proprietary and academic tools and simulators exist but with different formats, parameters, and levels of hierarchy. In order to support effective interdisciplinary research collaboration and enable tool interoperability, it is critical to develop standard interfaces across modeling abstraction layers including interchange formats, open-source libraries, and common metrics and benchmarks.

In turn, this is expected to have a strategic importance for education and training, an area in which a concrete goal has been identified at the workshop, namely, to realize an integrated design environment that would enable a team of students to design a heterogeneous system combining electronic with emerging interconnect technologies (such as nanophotonics and 3D integration) within three months.

3.4.2 Physical design models

The state of nanophotonic physical design models and simulation tools currently resembles the pre-Spice era of electronic design. Field-solvers and semiconductor device

simulators are used to evaluate the performance of individual devices and no integration path exists to creating behavioral or compact models in an automated way, compatible with standard circuit simulators and EDA environment. Often, manual behavioral model generation is used based on first-principles, i.e., equation-based models and fitting parameters. Even this type of manual translation is at an early stage and plagued by convergence issues in modeling languages such as Verilog-A. Research in the following areas is needed to bridge this modeling gap:

- Development of mixed-domain (electro-optical) simulators
- Automated mixed-domain compact (parameterized) model generation methods for nanophotonic devices
- Development of systematic methodologies and a knowledge base for behavioral nanophotonic device modeling
- Incorporate engineered materials properties into Maxwell equation solvers to reflect near field interactions
- Develop device and component isolation strategies and models to assure robust operation at minimized footprint
- Incorporate the effect of electronic variations during computation on the performance of photonic circuits

Interfacing these novel physical design models of nanophotonics to the rest of the physical design EDA stack is crucial and integral to our aim towards cross-cut system modeling (Section 3.4.1).

The availability of these rigorous design tools would also enhance the understanding of the reliability of the larger-scale nanophotonic systems, which is a concern that often arises as a barrier to adoption of the photonic technologies. The key focus here is on the failure mechanism analysis at different levels of granularity and design hierarchy, from the device level (device failure modeling, mitigation, effects on large systems) to the system level (BER and ECC codes and their performance/cost trade-offs).

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6. Additional Workshop Information

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