

ANALOG VERY LARGE SCALE INTEGRATED CIRCUITS DESIGN  
OF TWO-PHASE AND MULTI-PHASE VOLTAGE DOUBLERS  
WITH FREQUENCY REGULATION

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THIS THESIS ENTITLED  
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has been approved

for the School of Electrical Engineering and Computer Science  
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## Chapter 1

### INTRODUCTION

The purpose of this thesis is to implement two charge pump circuits based on voltage doubler into integrated circuits. Based on the Makowski charge pump and Starzyk charge pump, a TPMM (Two-Phase Makowski Multipliers) and a MPVD (Multi-Phase Voltage Doublers) are designed and implemented into the Orbit 2.0 $\mu$ m analog CMOS technology. Several additional circuits are designed to make these charge pumps work properly. Two frequency regulator circuits are designed to improve the power efficiencies. The driving abilities and the power are discussed in detail. Both the simulation results and the test reports of the sample chips are presented and compared.

#### 1.1 Overview of Various Charge Pumps

The charge pump is used to provide voltage different from the power supply. A DC-DC charge pump provides a DC voltage that is higher than the DC voltage of the power supply or provides a voltage of a reverse polarity. Compared to power converters with inductive energy storage components, charge pumps use no magnetic components. Hence, it is feasible to implement them in single IC chips. The voltage gains are obtained in a charge pump as a result of transferring charges to a capacitive load not involving amplifiers or transformers; thus the applications of charge pumps are limited mainly to a low power level [1].

Charge pumps can be used in various applications, such as analog switches [2] [3], op-amp power supplies [4], flash EEPROMs [5]-[10], continuous time filters [11], etc. where a higher or inverse voltage level is needed from a power source.

There exists various charge pumps -- among them, Dickson [12]-[14] and Makowski [15] [16] charge pumps are the two most efficiently and widely used designs. A Dickson charge pump uses a diode chain coupled to the inputs via capacitors, and a two-phase clock is used to control the charge transferring between capacitors. A higher than power supply voltage is achieved by successively transferring the packets of charge along the diode chain.

The Makowski charge pump is based on the voltage multiplier circuit. In [15], Makowski established a theoretical limit on the voltage gain in a two-phase multiplier and related it to Fibonacci numbers. Makowski's charge pumps have the highest voltage gains that need the least number of capacitors among two-phase charge pumps.

Both Dickson and Makowski charge pumps need two-phase clocks. Starzyk proposed a newly designed multi-phase charge pump [17], which requires more than two-phase clocks and is based on a voltage doubler [18]. To achieve the same voltage gain Starzyk charge pump uses fewer capacitors than does the Makowski charge pump.

## 1.2 Introduction to Voltage Doubler

A switched-capacitor organization of a two-phase DC-DC voltage doubler is shown in Figure 1-1. It contains two clock-controlled switches and two capacitors.  $V_{IN}$  is the power supply and  $V_+$  the voltage output. For a simple explanation of the voltage doubler operation, let us assume that the switches and the capacitors are all ideal. That is, we assume that there is no leakage current in the capacitors and that the electric charge transferring is instantaneous. Let us also assume that the voltage doubler starts in Phase I. The capacitor  $C1$  is initially charged by the power source to a voltage  $V_{IN}$ , and  $C_L$  is assumed to have no initial charge. In Phase II, the lower voltage terminal  $C1^-$  of  $C1$  is connected to the power supply. If there were no  $C_L$  connected to the higher voltage terminal  $C1^+$ ,  $C1^+$  would have a voltage of value  $2 \cdot V_{IN}$ . As the  $C1^+$  is connected to  $C_L$ , the charge stored in  $C1$  is shared with  $C_L$ . The final output voltage  $V_+$  is fixed by the

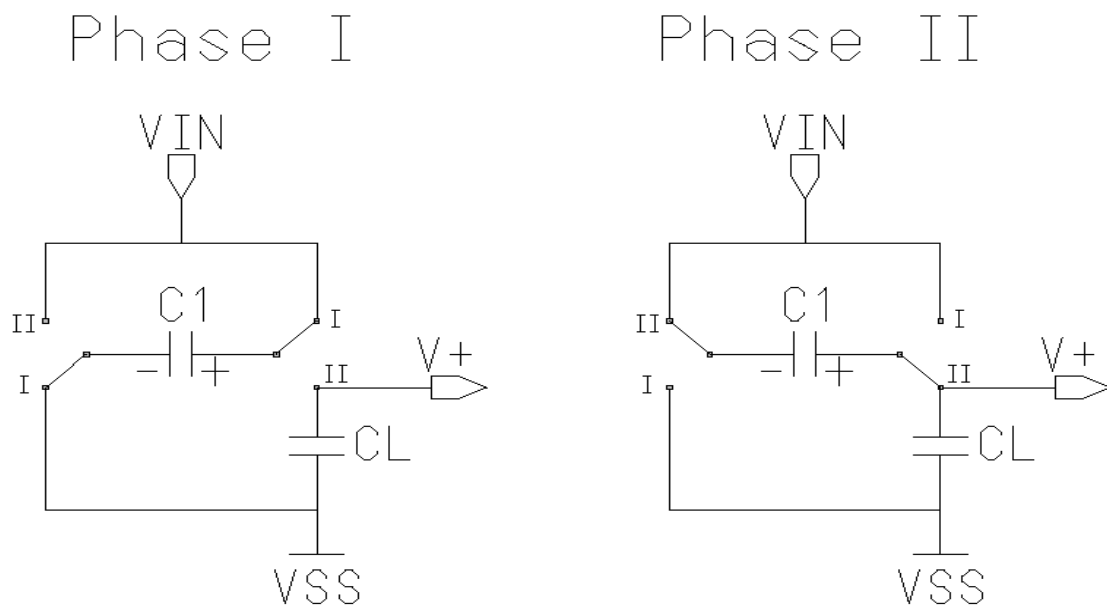


Figure 1-1: Voltage Doubler

VIN plus a voltage due to the final charge in the capacitor C1. This charge is less than the initial one in Phase I. The charge redistribution allows V+ to grow. Subsequently, the voltage doubler goes back to Phase I, C1 is recharged to hold a voltage VIN, and CL keeps the previous charge. Then the circuit is switched to Phase II again. We obtain a final output voltage V+ of value greater than the previous one due to the charge stored in CL. By repeating these operations many times, the output voltage V+ keeps growing to a higher voltage level.

Let us consider the charge redistribution between C1 and CL during nth clock period. Assuming that V+ is charged to V<sub>n-1</sub> after n-1 clock periods and that the final V+ in nth clock period is V<sub>n</sub>, we have

$$C1 \times VIN + CL \times V_{n-1} = C1 \times (V_n - VIN) + CL \times V_n \quad (1-1)$$

$$V_n = \mathbf{a} \times V_{n-1} + \mathbf{b} \times VIN \quad (1-2)$$

$$\text{where } \mathbf{a} = \frac{C1}{C1 + CL}, \quad \mathbf{b} = \frac{2 \times CL}{C1 + CL}.$$

By assuming the initial value of V+ is 0V, after pumping n period, the final output voltage V+ is given by

$$V_n = \frac{1 - \mathbf{a}^n}{1 - \mathbf{a}} \mathbf{b} \times VIN = 2 \times (1 - \mathbf{a}^n) \times VIN \quad (1-3)$$

When  $n \rightarrow \infty$ , since  $0 < \alpha < 1$ , the item  $1 - \alpha^n$  tends to 1, so the final voltage output V+ equals to  $2 \times VIN$ .  $\alpha$  is the factor which affects the "pumping speed" to reach the final voltage value. The larger the ratio of C1/CL, the larger value of  $\alpha$ ; thus, the V+ increases quickly to the final value.

In real application, the voltage doubler is used to provide higher voltage than the power supply and it has a load circuit. For simple analysis, we use a resistor  $R_L$  to represent the load circuit, as shown in Figure 1-2. Since the charge delivered to  $C_L$  from  $V_{IN}$  is partly consumed in  $R_L$ , the final output voltage  $V_+$  cannot reach  $2 \cdot V_{IN}$  as in the ideal condition.

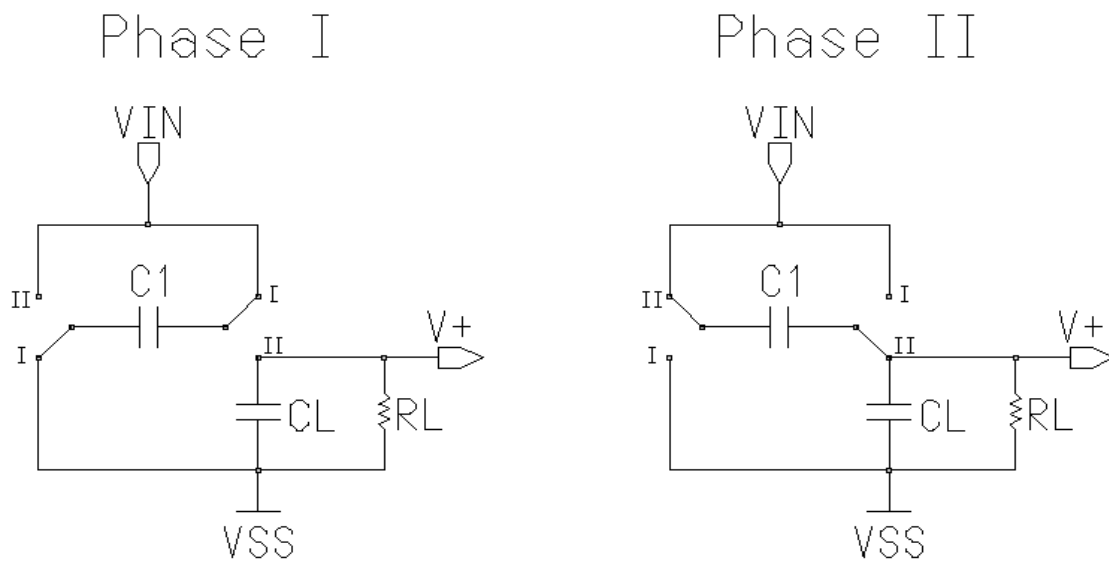


Figure 1-2: Voltage Doubler with Load Resistor

Let us analyze the final output voltage and driving ability of the voltage doubler with load resistor. After pumping many times, it comes to a steady state in which the charge delivered from the power supply,  $V_{IN}$ , equals to the charge consumed in  $R_L$ . In Phase I, the voltage on  $C_1$  changes from  $V_{1low}$  to  $V_{IN}$ , and  $V_+$  changes from  $V_{2high}$  to  $V_{2low}$  to supply the charge consumed in  $R_L$ . Let us assume the average voltage of  $V_+$  is half the sum of  $V_{2high}$  and  $V_{2low}$  and the voltage doubler works at clock period  $T$ . Then the average current  $I_{load}$  on  $R_L$  is  $(V_{2high} + V_{2low})/2R_L$  and the charge consumed in Phase I

equal to  $I_{load}$  times half clock period. In Phase II, the voltage on CL is changed back to  $V_{2high}$  and voltage on C1 changes to  $V_{1low}$  to support the resistor load and deliver the charge to CL and we get

$$CL \times (V_{2high} - V_{2low}) = \frac{(V_{2high} + V_{2low}) \times T}{4 \times RL} \quad (1-4)$$

$$C1 \times VIN + CL \times V_{2low} = C1 \times V_{1low} + CL \times V_{2high} + \frac{(V_{2high} + V_{2low}) \times T}{4 \times RL} \quad (1-5)$$

$$V_{2high} = VIN + V_{1low} \quad (1-6)$$

We can get the change and the average of  $V_+$  during one phase in steady state

$$\Delta V_+ = V_{2high} - V_{2low} = \frac{4 \times VIN}{1 + \frac{4 \times RL \times CL}{T} + \frac{4 \times CL}{C1}} \quad (1-7)$$

$$\overline{V_+} = \frac{V_{2high} + V_{2low}}{2} = \frac{2 \times VIN}{1 + \frac{T}{RL \times C1} + \frac{T}{4 \times RL \times CL}} \quad (1-8)$$

The variation of the output voltage  $V_+$  damages the characteristics of the output voltage and it should be reduced in application. According to Equation (1-7), we should select a larger value for CL and smaller value for C1 to get smaller change range of  $V_+$ .

Since we use the consistent load resistor RL to represent the load circuit, when  $V_+$  varies in a narrow range compared to the average  $V_+$ , the power output can be simply calculated as

$$\overline{P} \approx \frac{\overline{V_+}^2}{RL} = \frac{4 \times VIN^2}{\left(1 + \frac{T}{RL \times C1} + \frac{T}{4 \times RL \times CL}\right)^2 \times RL} \quad (1-9)$$

To achieve the higher output power -- in other words, to improve the driving ability of the voltage doubler -- we can select a smaller value for  $T$  and a larger value for  $C1$  and  $CL$ . After the  $VIN$ ,  $T$ ,  $C1$ , and  $CL$  are selected, there exists an optimum value for  $RL$  to achieve the maximum output power. The optimum load is given by

$$RL_{opt} = \frac{T}{C1} + \frac{T}{4 \times CL} \quad (1-10)$$

and the maximum power output is given by

$$\bar{P}_{max} = \frac{VIN^2}{\frac{T}{C1} + \frac{T}{4 \times CL}} \quad (1-11)$$

This result is achieved under the ideal condition that there is no leakage during the charge being delivered. For real implementation in analog CMOS technology, several factors reduce the driving ability to a much lower level. (This is discussed in detail in Chapter 2 and Chapter 3.)

### 1.3 Cascaded Voltage Doublers

To achieve a voltage gain higher than two, it is easiest to cascade the voltage doubler as shown in Figure 1-3. The output voltage of the previous voltage doubler is the power supply of the next voltage doubler. Similarly, by analyzing the circuit as was done for one-stage voltage doubler, it is reasonable to arrive at the result that the final output voltage is  $2^n$  times the voltage supply in ideal condition, where  $n$  is the number of stages of the charge pump. We can also see that every stage has two capacitors and two switches.

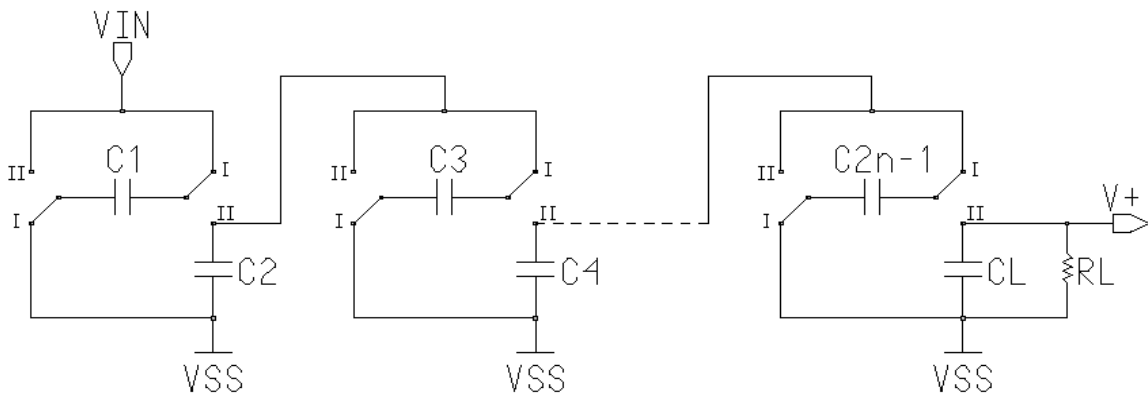


Figure 1-3: Two-Phase Voltage Doublers (Simply Cascaded)

Makowski proposed the highest voltage gain two-phase charge pump in [15]; the basic diagram of his charge pump is shown in Figure 1-4. The minimum number of stages required is two. Makowski presented this structure of a two-phase charge pump in more detail in [15] [16]. He established a theoretical limit on the voltage gain for any structure of in a two-phase charge pump. An  $n$ -stage, the Makowski charge pump has a voltage gain equal to this limit value which is equal to the  $2n$ th Fibonacci numbers 2, 5, 13, 34.... The Makowski charge pump has a higher voltage gain than that achieved by simply cascaded voltage doublers.

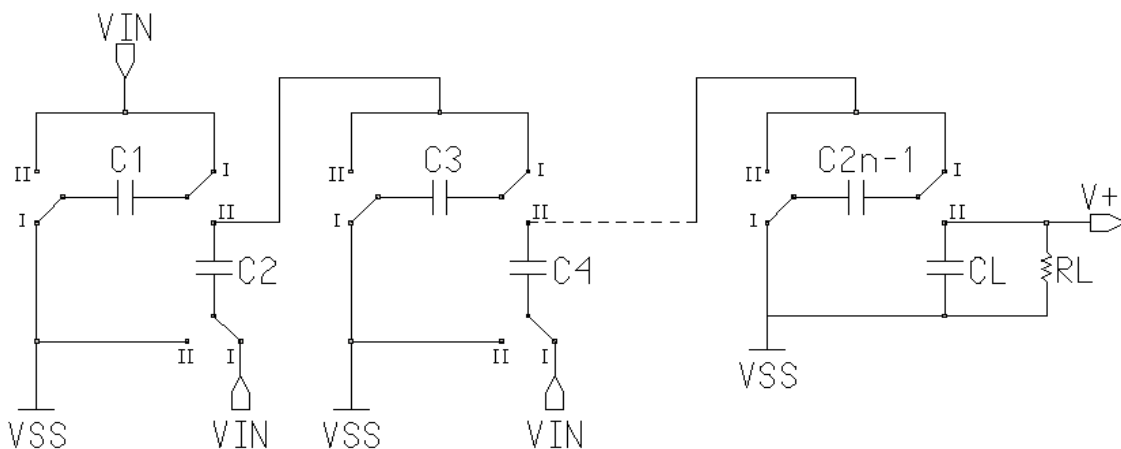


Figure 1-4: Two-Phase Makowski Multipliers



A new multi-phase charge pump proposed by Starzyk is shown in Figure 1-5. It requires  $n$  clock pairs to control the switches and it is also based on a voltage doubler. The minimum stage requirement is two stages. It can achieve the same voltage gain as the simply cascaded voltage doublers but uses less number of capacitors.

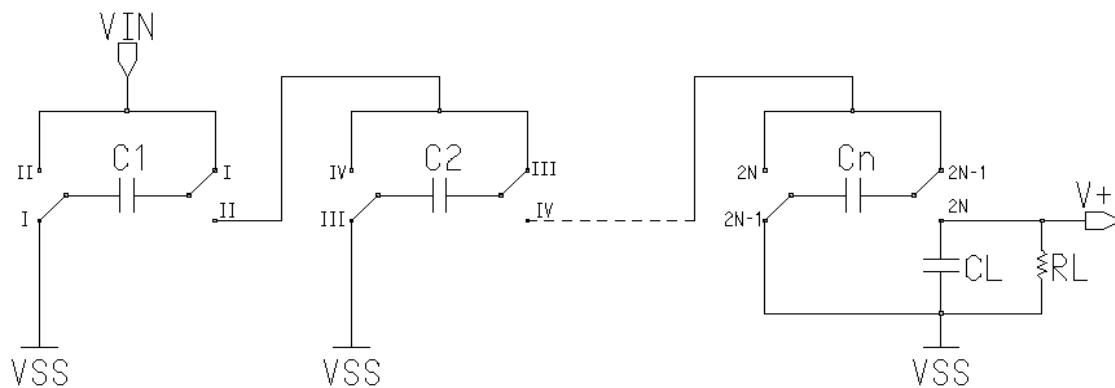


Figure 1-5: Multi-Phase Voltage Doublers (MPVD)

Table. 1-1 shows the comparison of these three charge pumps. All of them are assumed to be  $n$ -stage. We can see that the Starzyk charge pump needs  $n$  clock pairs and the others need only one clock pair, this makes the controlling circuit of the Starzyk charge pump much more complex. To implement the charge pump in a real circuit, the largest size is the capacitor; it uses a large area if implemented in IC and occupies a large space if implemented as a separate component. It is critical to use as fewer capacitors as possible in a charge pump circuits design. Among these three charge pumps, the Starzyk charge pump has the highest voltage gain if the same number of capacitors is used. Hence, a desired voltage gain can be implemented with the least design area.

Table 1-1: Comparison of three Charge Pumps

	Simply-cascaded	Makowski	Starzyk
Capacitors	$2n$	$2n$	$n+1$
Switches	$2n$	$3n-1$	$2n$
Clock pairs	1	1	$n$
Voltage gains	$2^n$	2nth Fibonacci	$2^n$

Based on the Makowski charge pump and Starzyk charge pump, a two-stage TPMM (Two-Phase Makowski Multipliers) and a two-stage MPVD (Multi-Phase Voltage Doublers) are designed. A frequency regulator [19] is used to lower the switching frequency when the load becomes lighter, thus reducing the power loss during switching. (This is discussed in detail in Chapter 4.) Both TPMM and MPVD are implemented in the SCNA Orbit [20]  $2.0\mu\text{m}$  analog CMOS technology by using the MOSIS fabrication services [21]. The schematic design, layout, and simulation results are achieved by using Mentor Graphics tools [22]. Chapter 2 introduces the schematic design of 2-stage TPMM and discusses its power driving ability and power efficiency in detail. Chapter 3 copes with MPVD. Chapter 4 presents the schematic, mechanism and simulation result for frequency converters. Chapter 5 covers the layout problems, and presents the simulation results for TPMM and MPVD with frequency converter. The measured results of these two charge pumps and conclusion are presented in Chapter 6.

## Chapter 2

### TWO-STAGE TPMM DESIGN

A two-stage TPMM (Two-Phase Makowski Multipliers) is designed and implemented into SCNA Orbit 2.0 $\mu$ m analog CMOS technology. This chapter discusses the schematic design, driving ability and the power efficiency of TPMM. The basic diagram of the designed two-stage TPMM is shown in Figure 2-1. It consists of two main parts -- one is the two-stage charging circuit that delivers charge to the load, and the other one is the clock pair generator, which generates the clock pair used to control switching of the charge pump. Power supply VIN (3.3V) and CLOCK (with frequency 20kHz) are assumed to be available for this TPMM. Input START is used to control starting/stopping of the charging process.

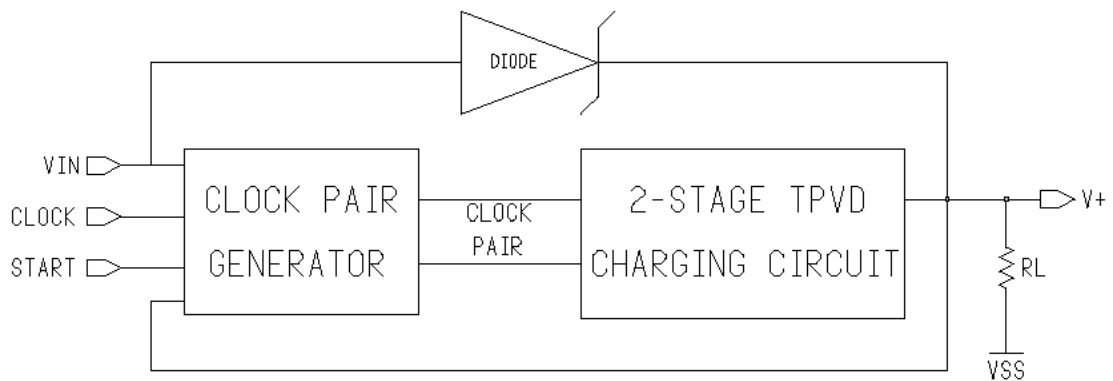


Figure 2-1: Diagram of Two-Stage TPMM

## 2.1 Two-Stage TPMM Charging Circuit

The schematic of the designed two-stage charging circuit is shown in Figure 2-2. Ten large MOS transistors are designed to control the connection and disconnection of the four capacitors -- C1, C2, C3, and CL. CK1 and CK2 work at 20kHz, they are used to switch these transistors on and off. The substrates of all the PMOS transistors are connected to V+, which is the highest voltage in the circuit. To turn these MOS transistors on and off properly, the clock pair should have amplitude of V+.

Let us assume that for these large transistors, the turned-off resistors are infinite and

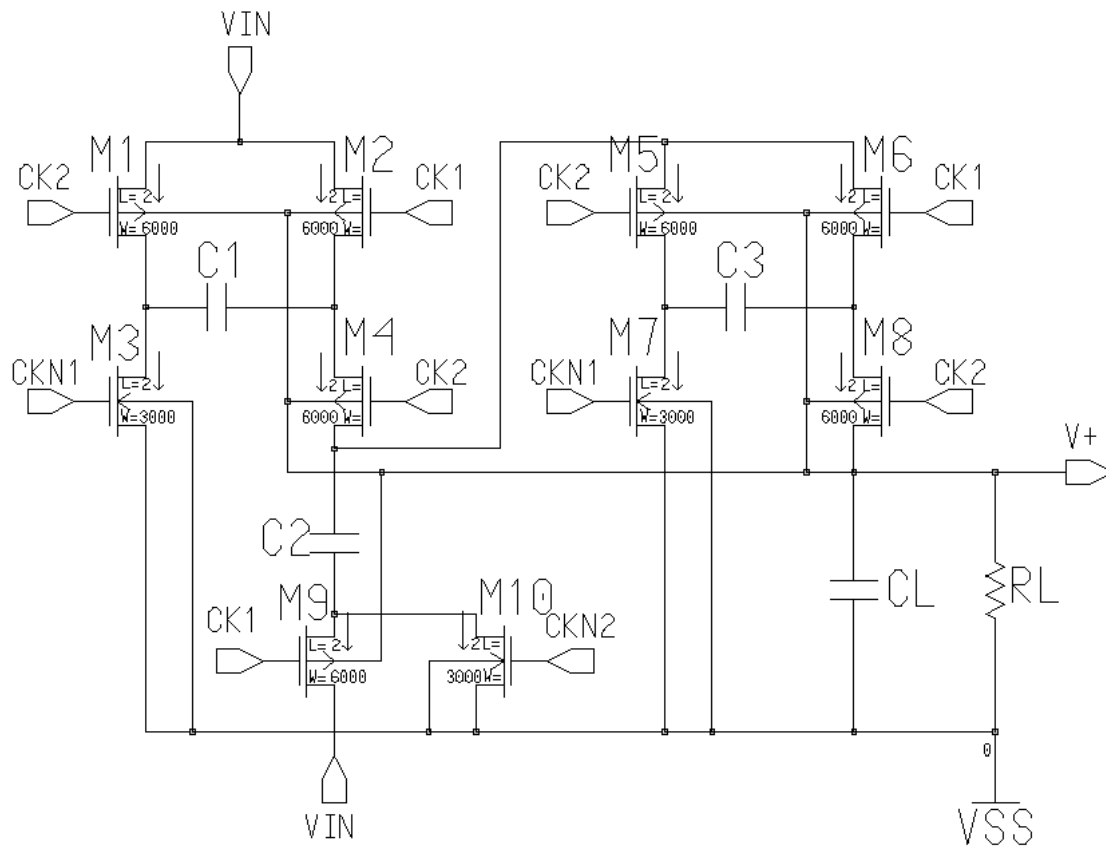


Figure 2-2: Two-Stage TPMM Charging Circuit

the turned-on resistors are zero in the ideal condition. There are two phases for TPMM, the ideal circuit for each phase is shown in Figure 2-3. Similar to the analysis of voltage doubler in Chapter 1, let us consider that after pumping many times, the TPMM comes to a steady-state that the charge delivered from power supply  $V_{IN}$  is equal to the charge consumed in  $RL$ .

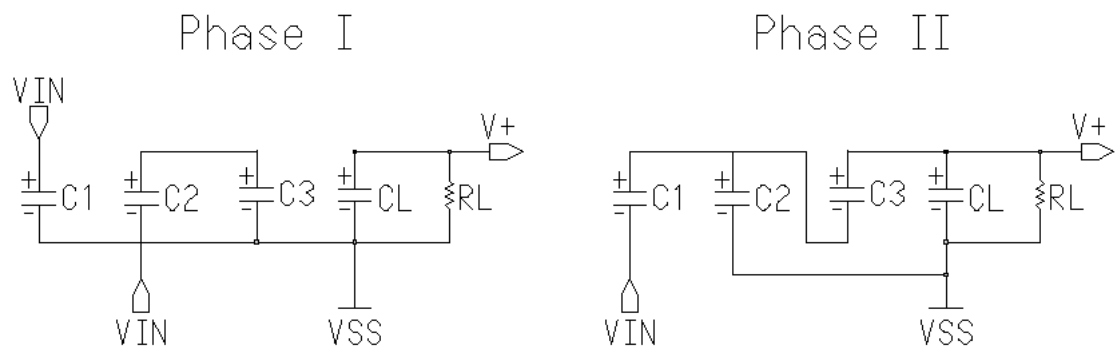


Figure 2-3: Ideal Circuits of Two-Stage TPMM

In Phase I,  $C1$  is charged from  $V_{1low}$  to  $V_{IN}$ ,  $CL$  supports  $RL$  and the voltage on it drops from  $V_{4high}$  to  $V_{4low}$ .  $V_{IN}$  is connected to  $C2-$  and there is charge redistribution between  $C2$  and  $C3$ , the voltage on  $C2$  changes from  $V_{2high}$  to  $V_{2low}$ , and the voltage on  $C3$  changes from  $V_{3low}$  to  $V_{3high}$ .

In Phase II,  $V_{IN}$  is connected to  $C1-$  to charge  $C2$  and then charge  $CL$  through  $C3$ . As the charge in  $C1$  is shared with  $C2$  and  $C3$ , the voltage on  $C1$  drops to  $V_{1low}$  and voltage on  $C2$  is charged to  $V_{2high}$ . Voltage on  $CL$  changes to  $V_{4high}$  and voltage on  $C3$  drops to  $V_{3low}$ . As we did in Chapter 1, let us assume the average voltage of  $V+$  is half of the sum of  $V_{4high}$  and  $V_{4low}$ ; then the average current on  $RL$  is  $(V_{4high} + V_{4low})/(2*RL)$ , and

the charge consumed in one phase is  $(V_{4high} + V_{4low}) \cdot T / (4 \cdot RL)$ . Assuming that there is no current leakage during switching, we have the following equations:

$$CL \times (V_{4high} - V_{4low}) = \frac{(V_{4high} + V_{4low}) \times T}{4 \times RL} \quad (2-1)$$

$$C3 \times (V_{3high} - V_{3low}) + CL \times (V_{4low} - V_{4high}) = \frac{(V_{4high} + V_{4low}) \times T}{4 \times RL} \quad (2-2)$$

$$C2 \times (V_{2high} - V_{2low}) + C3 \times (V_{3low} - V_{3high}) = 0 \quad (2-3)$$

$$C1 \times (VIN - V_{1low}) + C2 \times (V_{2low} - V_{2high}) + C3 \times (V_{3high} - V_{3low}) = 0 \quad (2-4)$$

$$VIN + V_{2low} = V_{3high} \quad (2-5)$$

$$VIN + V_{1low} = V_{2high} \quad (2-6)$$

$$VIN + V_{1low} + V_{3low} = V_{4high} \quad (2-7)$$

By solving these seven equations, we can get the average output voltage and the range that the output voltage varies. For this two-stage TPMM, I select the capacitors C1, C2, and C3 to have the same value  $C = 500\text{nF}$ . We can have the following results

$$\Delta V_+ = V_{4high} - V_{4low} = \frac{10 \times VIN}{\frac{4 \times RL \times CL}{T} + \frac{8 \times CL}{C} + 1} \quad (2-8)$$

$$\overline{V_+} = \frac{V_{2high} + V_{2low}}{2} = \frac{20 \times VIN}{4 + \frac{8 \times T}{RL \times C} + \frac{T}{RL \times CL}} \quad (2-9)$$

$$\overline{P_{out}} \approx \frac{\overline{V_+}^2}{RL} = \frac{400 \times VIN^2}{\left(4 + \frac{8 \times T}{RL \times C} + \frac{T}{RL \times CL}\right)^2 \times RL} \quad (2-10)$$

The average output voltage  $V_+$ , deviation  $\Delta V_+$ , and the average output power  $P_{out}$  depend on the load resistor  $R_L$ , after  $V_{IN}$ ,  $T$ ,  $C$  and  $CL$  are selected. To achieve the highest voltage, the optimum value for  $R_L$  and the maximum power output are given by

$$R_{L_{opt}} = \frac{2 \times T}{C} + \frac{T}{4 \times CL} \quad (2-11)$$

$$\bar{P}_{max} \approx \frac{\overline{V_+}^2}{R_L} = \frac{100 \times V_{IN}^2}{\frac{2 \times T}{C} + \frac{T}{4 \times CL}} \quad (2-12)$$

## 2.2 Clock Pair Generator

Figure 2-4 shows a block diagram of the clock pair generator. It contains a non-overlapping clock pair converter, two clock level shifters, and several buffer circuits. As shown in Figure 2-2,  $CK1$  and  $CK2$  control the switches of the large transistors. Ideally, if  $CK1$  is exactly the inverse of  $CK2$  and there is no delay in switching, the transistors

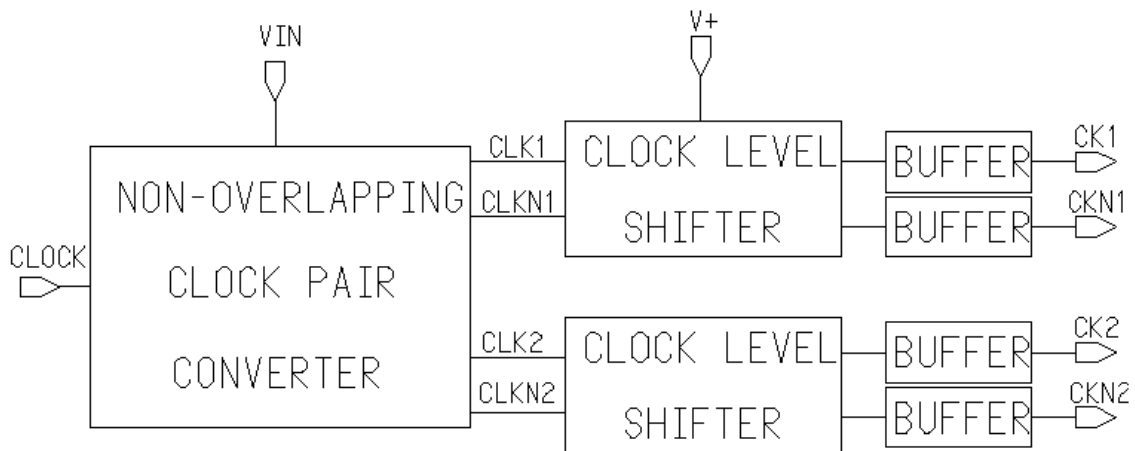


Figure 2-4: Clock Pair Generator

M1 and M2 shown in Figure 2-2 are not turned on at the same time. Since the W/L ratios of the transistors are selected to be very large (the reason is given in the section 2.4), the transistors' rise and fall times are very large. Subsequently, it takes a long time to turn these large transistors on and off. To avoid the situation in which both M1 and M3 enter the transition state, the clock pair CK1 and CK2 must be designed to guarantee that before M1 is turned on, M3 must be turned off completely, and vice versa. To make sure that there is no short circuit current and considering that a mismatch may occur during fabrication, the off-time (both CK1 and CK2 are low) should be several times larger than the rise time plus the fall time of the large transistors.

### **2.2.1 Non-Overlapping Clock Pair Generator**

The schematic of the non-overlapping clock generator is shown in Figure 2-5. The generated clock pair CLK1 and CLK2 with their inverse clock pair CLKN1 and CLKN2 is non-overlapping.

The RC-INV shown in Figure 2-6 is used to achieve the required delay. M1 is a PMOS transistor whose gate is connected to VSS, and it is kept in the turned-on state to work as a resistor. M2 is an NMOS that acts as a capacitor. These two transistors provide the required RC delay. The right two transistors (M3 and M4) act as the CMOS inverter. This RC-INV behaves as an inverter with long rise and fall time.

The simulation results of the non-overlapping clock generator reveal that the output clock pairs have the same period (50 $\mu$ s) as the input clock. The off-time is about 600ns. Compared to the clock period, the off-time is very small and does not affect the



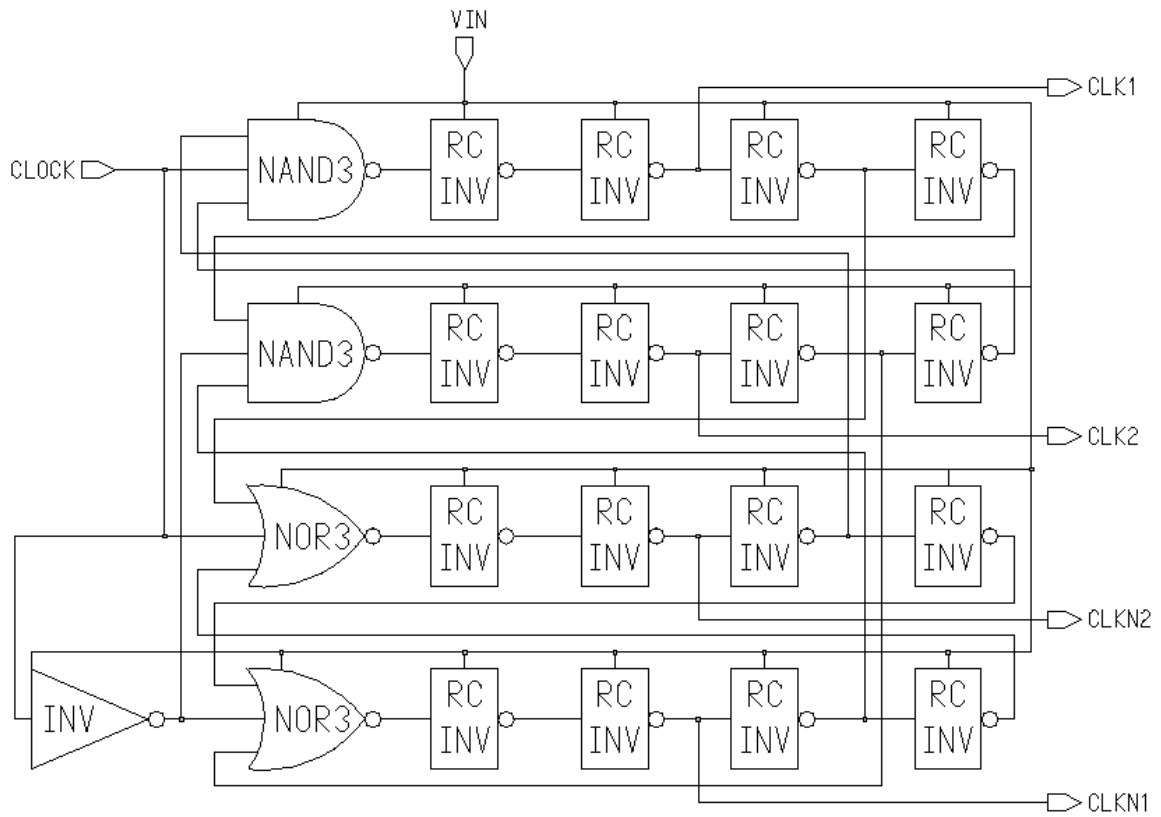


Figure 2-5: Non-Overlapping Clock Pair Generator

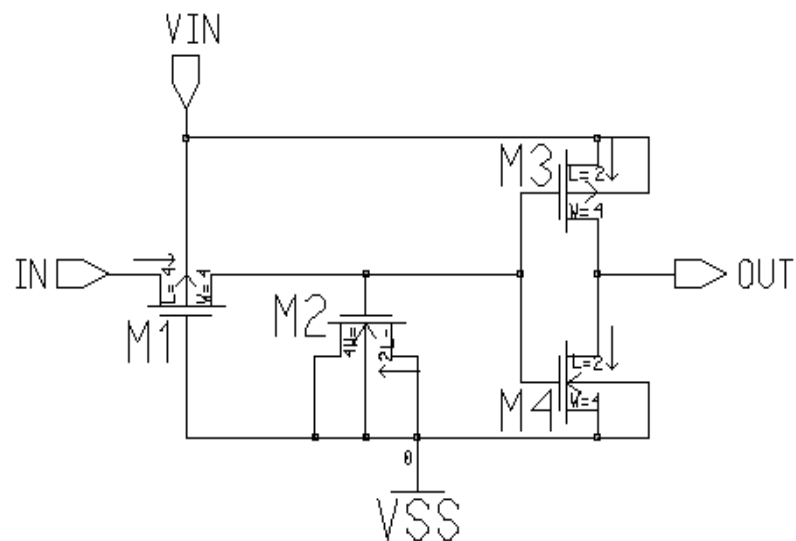


Figure 2-6: Schematic of RC-INV

clock characteristic. Meanwhile, the off-time is much larger than the rise and fall time of the large transistors (about 50ns) to avoid the short circuit current during switching.

### 2.2.2 Clock Level Shifter Design

As mentioned earlier, the substrates of all PMOS transistors are connected to  $V+$ . To turn the MOS transistors on and off properly, the controlling clock pairs should have amplitude of  $V+$ . A clock level shifter is designed to shift the clock level -- its schematic is shown in Figure 2-7. CLKN is the inverse of CLK,  $V+$  the output voltage of two-stage TPMM. By forcing  $V+$  to change from 3.3V to  $4 \times 3.3V = 16.5V$  for this TPMM, the simulation result of CKO is shown in Figure 2-8. It shows that CKO has the same phase as CLK, and CKO has amplitude of  $V+$ .

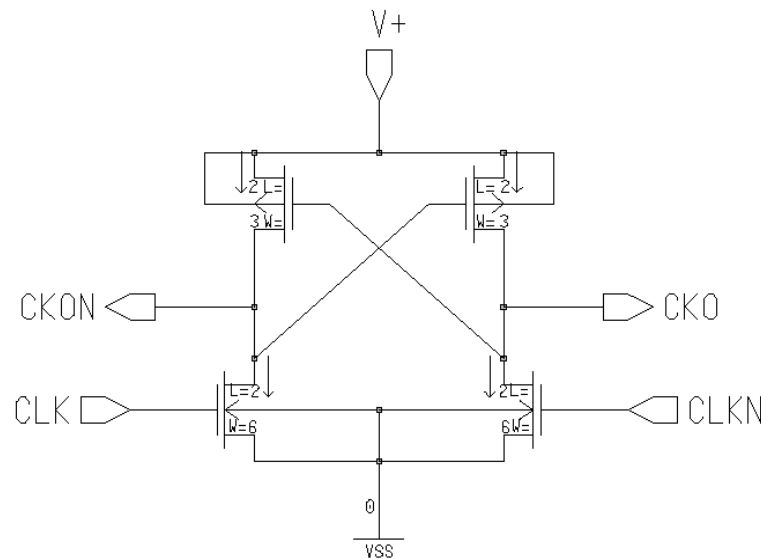


Figure 2-7: Clock Level Shifter

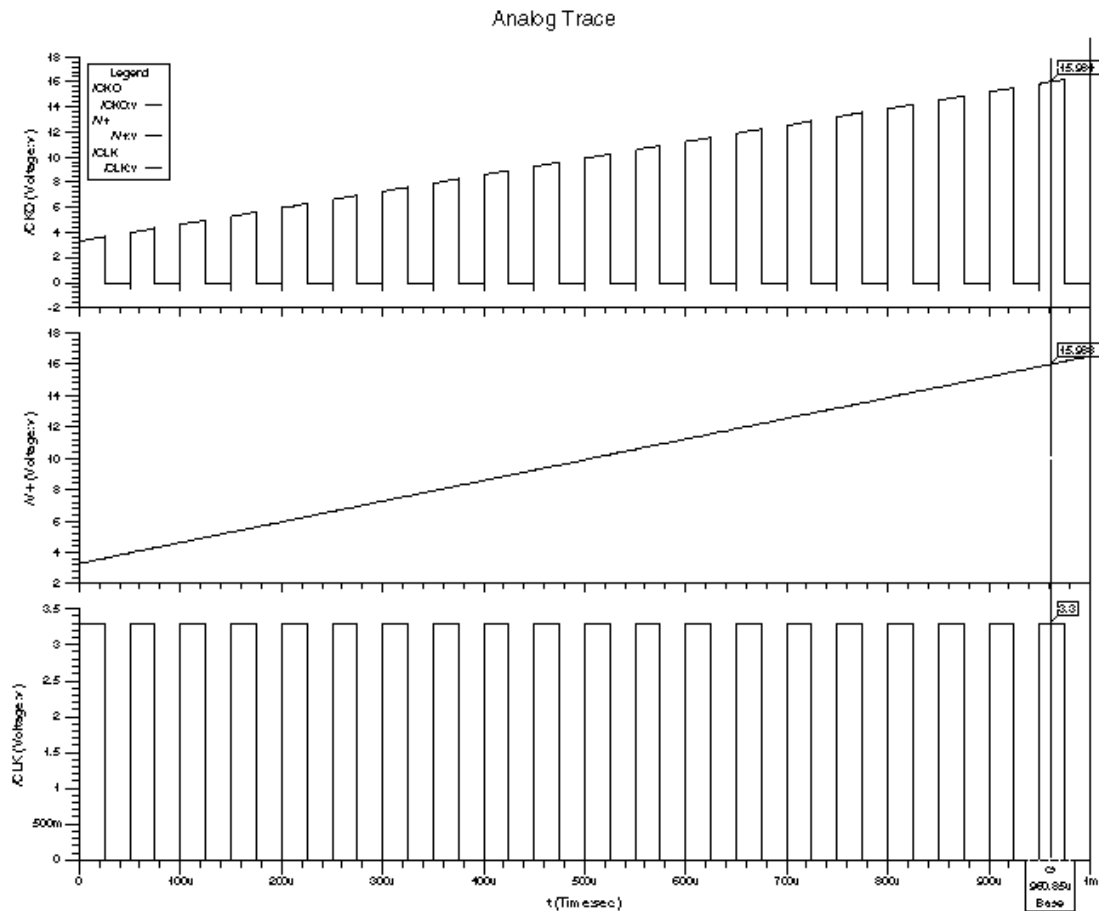


Figure 2-8: Simulation Result of Clock Level Shifter

### 2.2.3 Driving Buffers Design

The rise and fall time of these ten large transistors is very large. It takes a long time for the clock pair to drive these transistors directly, and there is a risk of a short circuit current during switching, even for 600ns off-time for the non-overlapping clock pair. To reduce the time spent in turning these transistors on and off, the driving buffer is designed, as shown in Figure 2-9. It contains three inverters with ratioed sizes -- OUT is

the inverse of IN. Simulation results reveal that the rise and fall time of the large transistors is dramatically reduced after the buffers are added to the circuit.

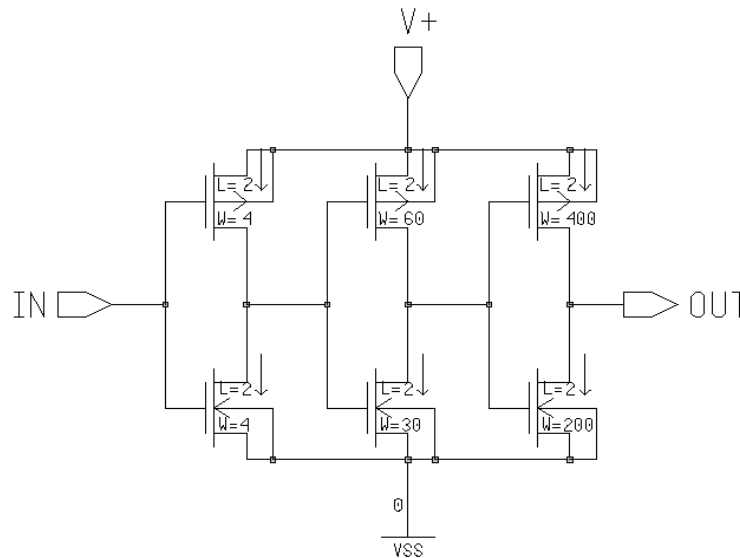


Figure 2-9: Driving Buffer

### 2.3 Start-Up Consideration

The controlling clock pair works with  $V+$  as logic 1 and  $VSS$  as logic 0 by using the clock level shifter. However, when the TPMM starts to pump, the initial value of  $V+$  is 0V, and after the clock pair is shifted to the initial  $V+$  level, the charging circuit does not work -- it latches up in the beginning. To avoid this condition, a diode is used to force the initial value for  $V+$ , as shown in Figure 2-1. It forces  $V+$  to have an initial value large enough to make the switching work. When  $V+$  is charged to be larger than  $V_{IN}$ , the diode has the reverse polarization and no energy is dissipated through the diode.

## 2.4 Pumping Efficiency of TPMM

We discussed the two-stage TPMM under an ideal condition. In a practical implementation, there is a power loss in delivering the charge from the power source to the load resistor. The power loss contains two components--resistive power loss and dynamic power loss. The resistive power loss occurs when the current goes through the large transistors, and most of the dynamic power loss occurs as a result of switching the large transistors. Some of the power loss transfers to heat that can harm the integrated circuit, and both conductive and dynamic power losses reduce the power efficiency; hence, it is very important to reduce the power loss to a minimum value for a desired output power.

### 2.4.1 Resistive Power Loss of TPMM

Figure 2-3 shows the ideal condition of the two-stage TPMM. To analyze the power loss in this circuit, the turned-on resistors of these large transistors cannot be neglected. The equivalent circuits are shown in Figure 2-10. The resistors  $R_1, R_2 \dots R_{10}$  represent the turned-on resistors of the large transistors  $M_1, M_2 \dots M_{10}$  (shown in Figure 2-3). When the circuit comes to the steady-state, the  $C_1, C_2, C_3$  and  $C_L$  are charged close to their final voltage level. In Phase I, the current  $i_1$  charges the capacitor  $C_1$  going from  $V_{IN}$  through  $R_2$  and  $R_3$  to  $V_{SS}$ ,  $i_2$  makes the charge redistribution between  $C_2$  and  $C_3$  and it goes from  $V_{IN}$  through  $R_9$  and  $R_6$  to  $V_{SS}$ . It is obvious that there is resistive power loss in resistors  $R_2, R_3, R_9$ , and  $R_6$  when charge is being delivered.

Similar results can be assumed for Phase II. The resistive power loss depends on the delivering current  $i_1$ ,  $i_2$ , and these turned-on resistors.

To reduce the resistive power loss, two obvious ways are to reduce the turned-on resistors and the delivering currents. Since the charge delivered by  $i_1$  and  $i_2$  is used to drive the load, the delivering currents  $i_1$  and  $i_2$  have the direct relationship to the load current. To keep the output power at a high level,  $i_1$  and  $i_2$  must have high values. The turned-on resistors depend on the ratio of the W/L of the transistors. To select the large ratio of W/L for these transistors results in small turned-on resistors, and thus saves power when delivering.

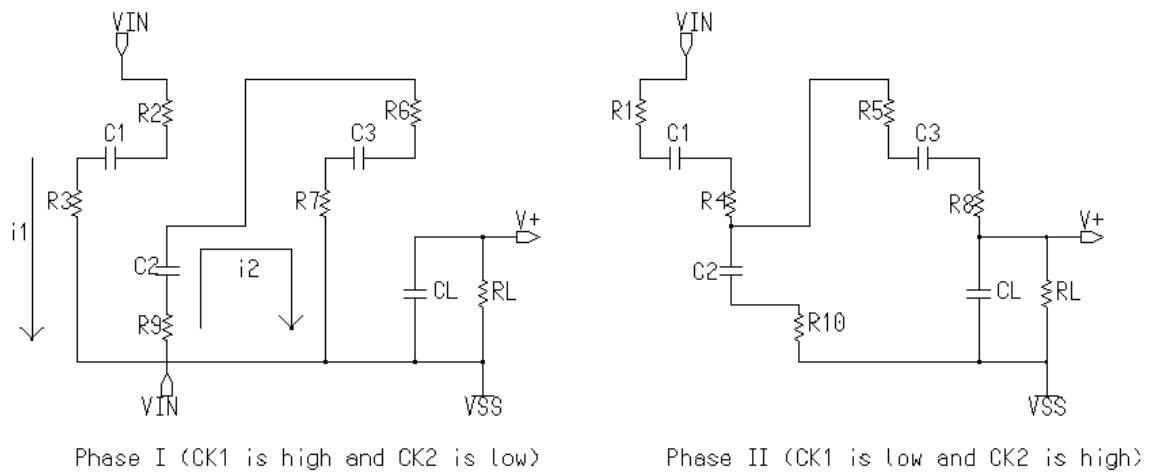


Figure 2-10: Equivalent Circuits of Two-Stage TPMM

### 2.4.2 Dynamic Power Loss of TPMM

There are two main components of the dynamic power losses in this TPMM. One is the power loss in charging and discharging the gates of the transistors; the other is the loss in diffusion capacitors of the source-bulk and the drain-bulk pn-junctions. Since the controlling clock pair CK1 and CK2 have the clock period  $T$  and amplitude  $V+$ , the switching power loss in gate capacitors  $P_g$  is given by (2-13), where  $C_{ox}$  is the gate capacitor per unit area of the transistors.

$$P_g = \frac{C_{ox} \times (V+)^2}{T} \times \sum_{i=1}^{10} W_i \times L_i \quad (2-13)$$

Let us check the source-bulk and the drain-bulk pn-junction of the TPMM, as shown in Figure 2-2. Every large transistor has one terminal (source or drain) kept at a constant voltage with the other terminal having a voltage level shifted during switching. These voltage level varying pn-junctions behave as capacitors and cause the dynamic power loss estimated by

$$P_{D/S} = (7 \times C_{PD/S} + 3 \times C_{ND/S}) \times \frac{VIN^2}{T} \quad (2-14)$$

where  $C_{PD/S}$  is the drain-bulk (source-bulk) diffusion capacitance of PMOS and  $C_{ND/S}$  is that of NMOS. The dynamic power loss is the sum of  $P_g$  and  $P_{D/S}$  and depends on the frequency and the value of  $W$  and  $L$  of the large transistors.

### 2.4.3 Power Efficiency of TPMM

The power loss is the sum of conduction power and dynamic power loss. Let us assume the output power is  $P_{out}$ . Then the power efficiency for this charge pump is given by

$$f_P = P_{out} / (P_{out} + P_R + P_g + P_{D/S}) \quad (2-15)$$

To achieve higher pumping efficiency, both resistive and dynamic power losses should be reduced. As discussed earlier, the ratio of W/L should be large to reduce resistive power loss, and the product W\*L should be small to reduce the dynamic power. L is set to the minimum size of 2.0  $\mu\text{m}$  required by SCNA Orbits design rule. Then W can be designed to minimize both resistive power loss and dynamic power loss. The optimized W is equal to 3000  $\mu\text{m}$  for NMOS and 6000  $\mu\text{m}$  for PMOS.



## Chapter 3

### TWO-STAGE MPVD DESIGN

Similar to the two-stage TPMM, a two-stage MPVD is designed and implemented to SCNA Orbit 2.0  $\mu\text{m}$  analog CMOS technology. This chapter presents the schematic design consideration of MPVD, the power efficiency is also discussed. The designed MPVD shown in Figure 3-1 consists of two main parts--the two-stage MPVD charging circuit and the clock pairs generator, which generates two non-overlapping clock pairs to control the switches. VIN (3.3V) and CLOCK (20kHz) are selected to have the same value as the TPMM.

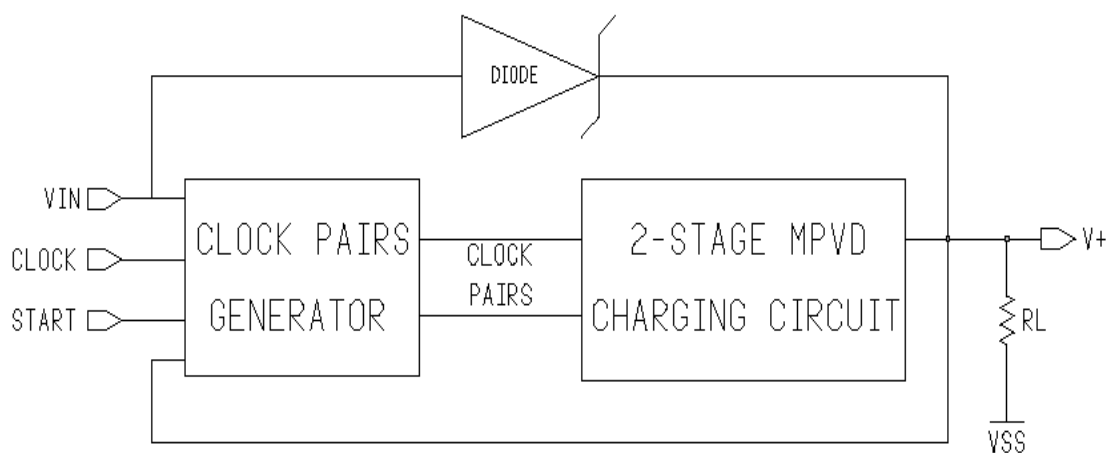


Figure 3-1. Diagram of Two-Stage MPVD



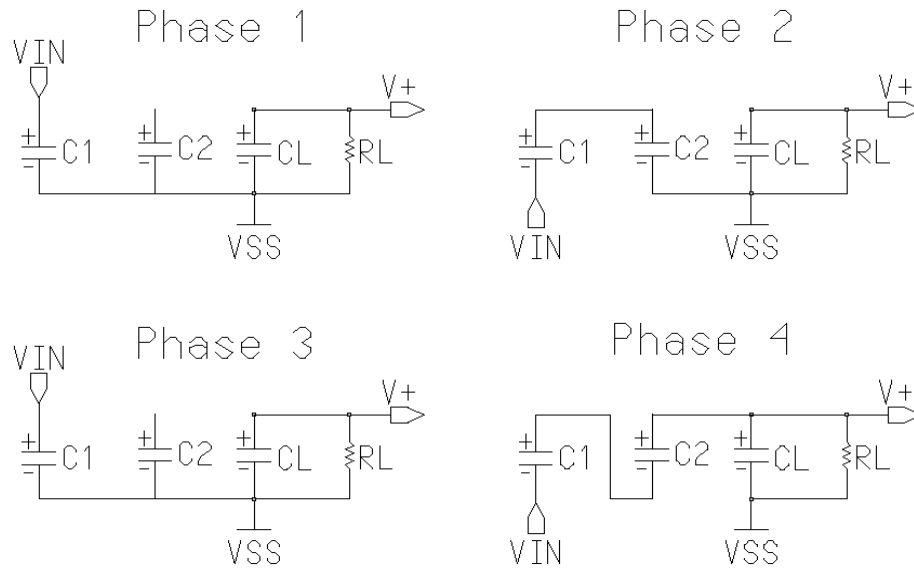


Figure 3-3: Ideal Circuits of Two-Stage MPVD

We use  $V_{ij}$  to represent the final voltage on capacitor  $j$  (1 for  $C1$ , 2 for  $C2$ , and 3 for  $CL$ ) in Phase  $i$ . The  $V_+$  is always connected to the terminal  $CL_+$ ,  $CL$  supports the output power in the Phase 1, 2 and 3 independently. In Phase 4,  $CL$  is charged from its lowest value  $V_{33}$  to its highest value  $V_{34}$ . Let us assume that the average voltage of  $V_+$  is the average of  $V_{33}$  and  $V_{34}$ , the charge consumed in every phase (one-fourth clock period) is

$\frac{(V_{33} + V_{34})}{2 \times RL} \times \frac{T}{4}$ . Similar to the analysis of TPMM, we have the following equations

$$V_{11} = V_{13} = VIN \quad (3-1)$$

$$VIN + V_{12} = V_{22} \quad (3-2)$$

$$VIN + V_{14} + V_{24} = V_{34} \quad (3-3)$$

$$V_{21} = V_{24} \quad (3-4)$$

$$V_{23} = V_{22} \quad (3-5)$$

$$C1 \times (V_{12} - V_{11}) + C2 \times (V_{22} - V_{21}) = 0 \quad (3-6)$$

$$C1 \times (V_{14} - V_{13}) - C2 \times (V_{24} - V_{23}) = 0 \quad (3-7)$$

$$C2 \times (V_{24} - V_{23}) + CL \times (V_{34} - V_{33}) = \frac{(V_{33} + V_{34}) \times T}{8 \times RL} \quad (3-8)$$

$$CL \times (V_{34} - V_{31}) = CL \times (V_{31} - V_{32}) \quad (3-9)$$

$$CL \times (V_{31} - V_{32}) = CL \times (V_{32} - V_{33}) \quad (3-10)$$

$$CL \times (V_{32} - V_{33}) = \frac{(V_{33} + V_{34}) \times T}{8 \times RL} \quad (3-11)$$

By selecting  $C1 = C2 = C$ , we can have the results

$$\Delta V_+ = V_{34} - V_{33} = \frac{8 \times VIN}{1 + \frac{8 \times RL \times CL}{3 \times T} + \frac{4 \times CL}{C}} \quad (3-12)$$

$$\overline{V_+} = \frac{V_{34} + V_{33}}{2} = \frac{4 \times VIN}{(1 + \frac{3 \times T}{2 \times RL \times C} + \frac{3 \times T}{8 \times RL \times CL})^2 \times RL} \quad (3-13)$$

$$\overline{P} \approx \frac{\overline{V_+}^2}{RL} = \frac{16 \times VIN^2}{(1 + \frac{3 \times T}{2 \times C \times RL} + \frac{3 \times T}{8 \times CL \times RL})^2 \times RL} \quad (3-14)$$

The range of  $V_+$  depends on the ratio of  $C/CL$ --to make the output voltage steady,  $C/CL$  should be small. When  $RL \rightarrow \infty$ , the output voltage has its highest value  $4 \times VIN$ . The output power depends on  $RL$ . The optimum value for  $RL$  and the maximum power output are given by the following equations:

$$RL_{opt} = \frac{3 \times T}{2 \times C} + \frac{3 \times T}{8 \times CL} = \frac{3 \times T}{2} \left( \frac{1}{C} + \frac{1}{4 \times CL} \right) \quad (3-15)$$

$$\bar{P}_{\max} = \frac{8 \times V_{IN}^2}{3 \times \left( \frac{1}{C} + \frac{1}{4 \times CL} \right)} \quad (3-16)$$

Similar to the analysis of the TPMM, equation (3-16) shows that the larger the value of T, the larger the output power. Both C and CL are the important positive factors for the driving ability, therefore, C and CL should be large to drive a heavier load.

### 3.2 Clock Pairs Generator

Figure 3-4 shows the diagram of the clock pairs generator, which contains a T flip-flop (TFF), non-overlapping clock pairs converter, level shifters, and several buffer circuits.

Similar to the TPMM, the non-overlapping clock pairs converter is used to generate non-overlapping clock pairs to avoid a short circuit current. Since there are four

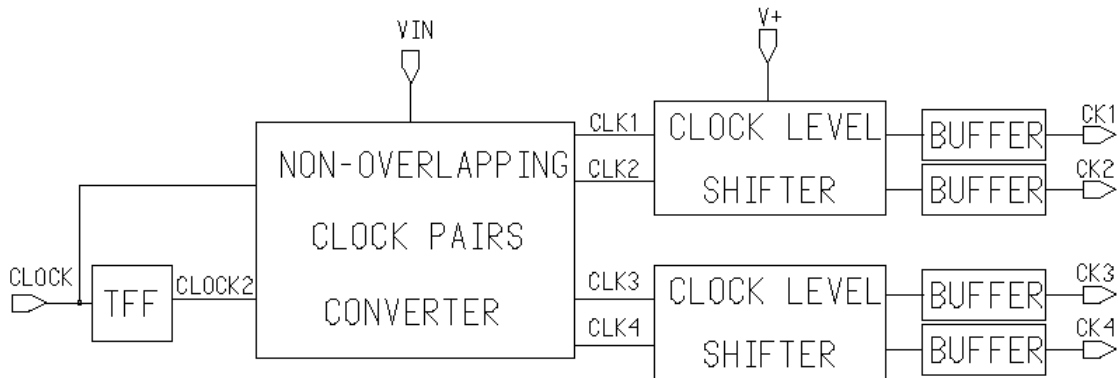


Figure 3-4: Clock Pairs Generator

phases for MPVD, we must convert two clock pairs to non-overlapping. To turn the large MOS transistors on and off properly the clock level shifters are designed to shift the clock pairs to have amplitude of V+. The buffers are used to shorten the rise and fall time

of the large transistors. The diode shown in Figure 3-1 is used to initialize  $V+$  to avoid the latch-up when starting.

As mentioned earlier, a two-stage MPVD uses two clock pairs to control the switching of these capacitors, as shown in Figure 3-2. CK1 and CK2 have the same frequency of CLOCK. CK3 and CK4 have half the frequency of CLOCK. A T flip flop is used to achieve CLOCK2 with the half frequency of CLOCK. The schematic of TFF is shown in Figure 3-5 and the simulation result is shown in Figure 3-6. The outputs Q and QN have the clock period  $100\mu\text{s}$ , which is two times of CLOCK ( $50\mu\text{s}$ ).

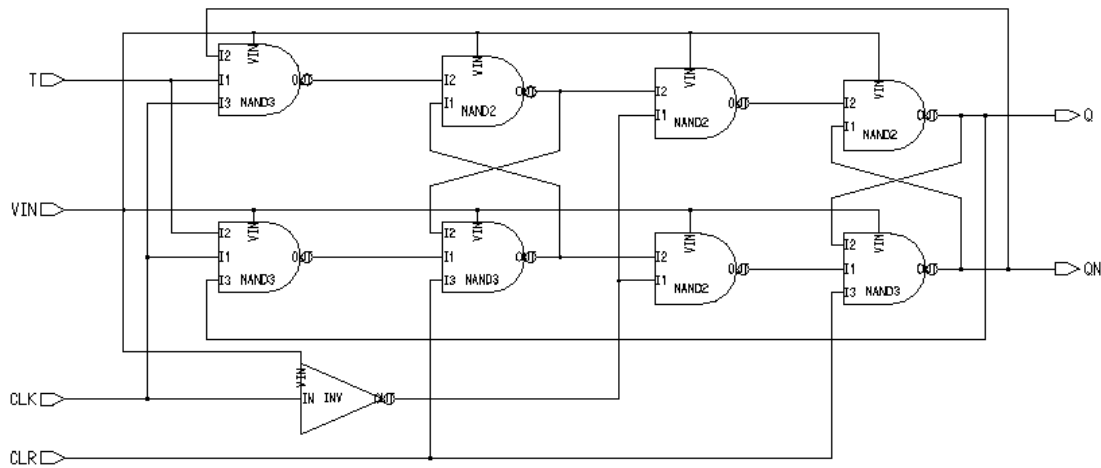


Figure 3-5: TFF ( T Flip Flop )

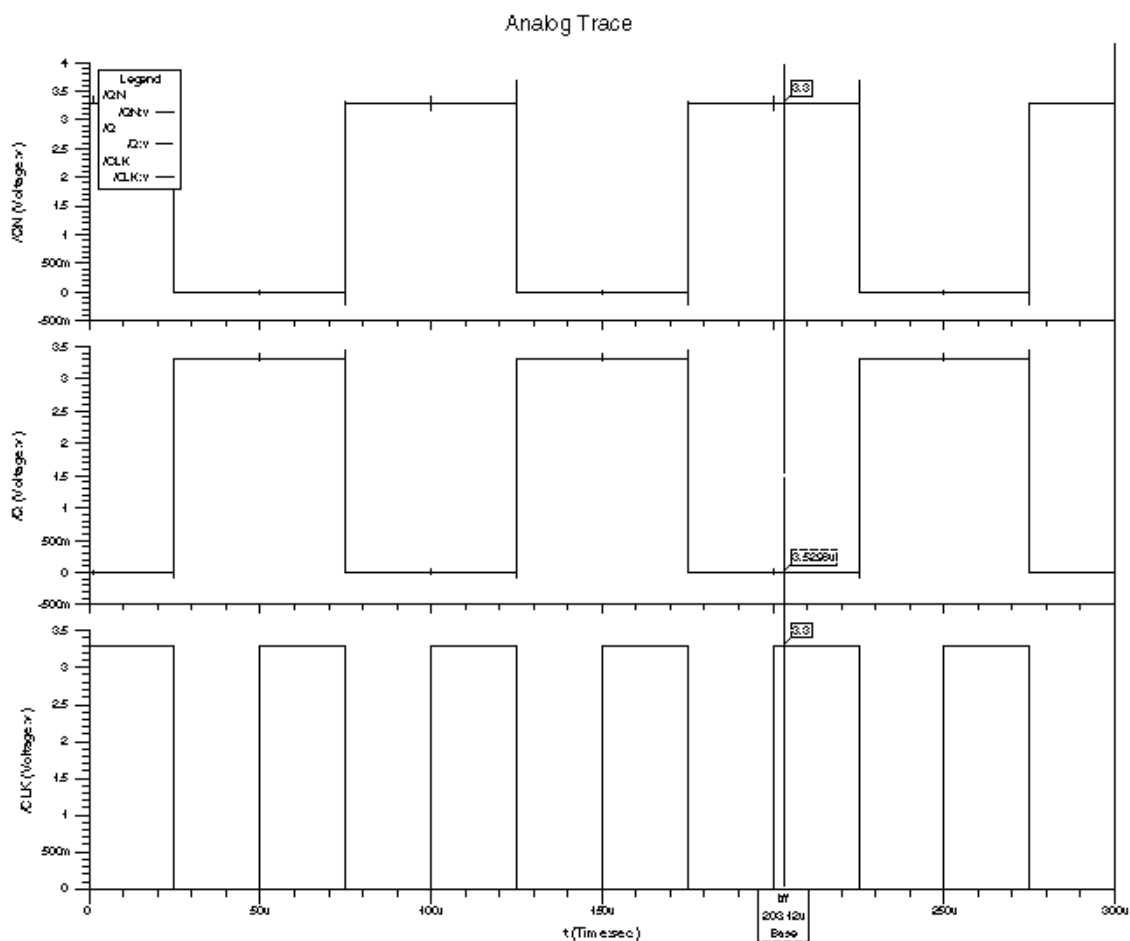


Figure 3-6: Simulation Result of TFF

### 3.3 Pumping Efficiency of MPVD

Figure 3-3 shows the ideal circuit of a two-stage MPVD. In practical implementation, the MPVD has resistive power loss and dynamic power losses as a TPMM dose. The equivalent circuit of two-stage MPVD is shown in Figure 3-7. The turned-on transistor R1, R2, ... R8 consumes the power when the charge is delivered through the transistors. We can select the large ratio of W/L for the transistors to reduce the turned-on resistor thus, and to reduce the resistive power loss.

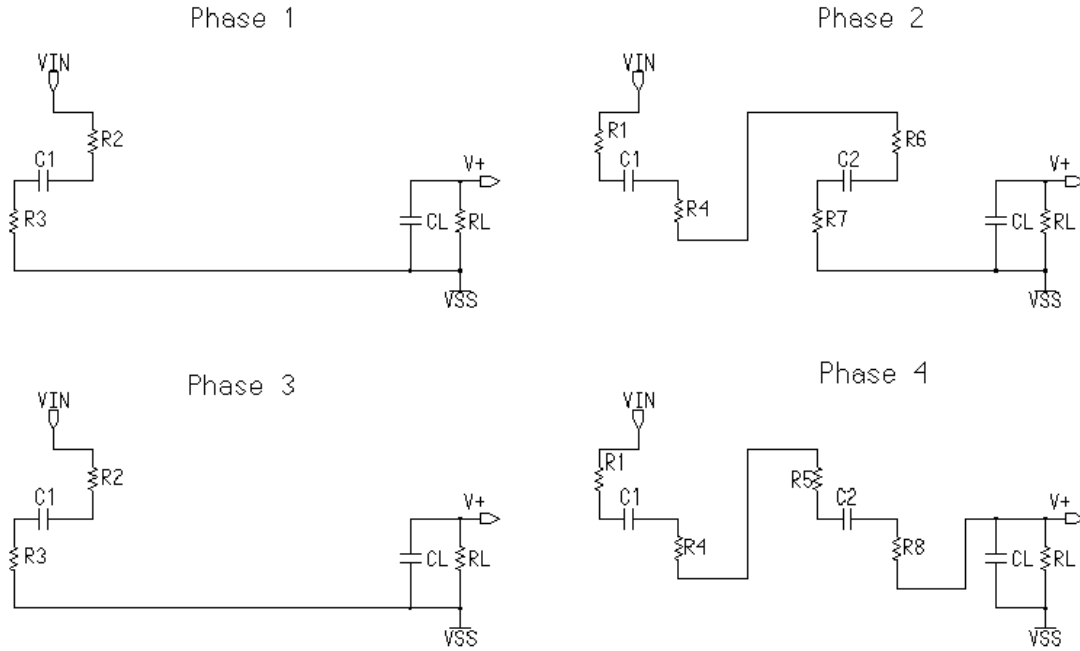


Figure 3-7: Equivalent Circuits of Two-Stage MPVD

There are two main dynamic power losses in this two-stage MPVD during switching. One is the power loss in the MOSs' gates. Since the controlling clock pairs CK1 and CK2 have the clock period  $T$  ( $50\mu\text{s}$ ) and CK3 and CK4 have the clock period  $2T$  (all of them have an amplitude of  $V+$ ), the switching power loss in the gate capacitors  $P_g$  is given by

$$P_g = \frac{C_{ox} \times (V+)^2}{T} \sum_{i=1}^4 W_i \times L_i + \frac{C_{ox} \times (V+)^2}{2 \times T} \sum_{j=5}^8 W_j \times L_j \quad (3-17)$$

The other power loss is the loss in diffusion capacitors of the source-bulk and the drain-bulk pn-junctions. Let us analyze the source-bulk and the drain-bulk pn-junction of the MPVD, as shown in Figure 3-2, as we did for TPVD. Every large transistor has one



terminal (source or drain) kept at a constant voltage, and the other terminal has a voltage level which shifts during switching. They cause the dynamic power loss estimated by

$$P_{D/S} = (9 \times C_{PD/S} + 3 \times C_{ND/S}) \frac{VIN}{T} \quad (3-18)$$

Both of the  $P_g$  and  $P_{D/S}$  depend on the switching frequency and the value of  $W$  and  $L$  of the large transistors.

Power efficiency depends on the power output, resistive, and dynamic power loss. To get the higher power efficiency, both resistive and dynamic power losses should be reduced. Similar to TPMM, we set  $L$  to the minimum size of  $2.0 \mu\text{m}$  required by SCNA Orbits design rule.  $W$  equals to  $3000 \mu\text{m}$  for NMOS and  $6000 \mu\text{m}$  for PMOS.

When the load becomes lighter with less charge consumed in  $RL$ , the current through the transistors decreases, which reduces the resistive power loss. The factors affecting the dynamic power loss do not change. Since the power output is decreased due to the lighter load, the ratio of the power loss over the power output increases, which reduces the pumping efficiency. Especially for the no-load condition, the charge pump still wastes a large amount of power, and the power efficiency is 0%. To avoid this situation, the switching frequency must be lowered when the load becomes lighter. This problem is solved in chapter 4.

## Chapter 4

### FREQUENCY CONVERTER DESIGN

#### 4.1 Structures of the Frequency Converters

As discussed in Chapter 3, the power efficiency of the charge pump changes when the load changes. When the load becomes very light, the power efficiency decreases dramatically. Especially under the no load condition, the charge pump also needs to deliver the power to keep it working even the power efficiency is zero. In a real application, it is necessary to keep the high output voltage, but unnecessary to drive a heavy load all the time. Hence, it is necessary to lower the switching frequency, and thus, reduce the power loss for the lighter load--especially for the no load condition.

As the load becomes lighter, the charge delivered to the load becomes smaller, the resistive power loss is reduced, and the dynamic power does not change along with the load. We can see that most of the power loss is due to dynamic power loss when the load becomes lighter. Let us consider Equations (2-13) and (2-14). Since  $V_{IN}$ ,  $W$ , and  $L$  are fixed after design, the only factor that can be used to feedback is  $T$  (or the frequency  $f$ ). According to Equation (2-9), when the load becomes lighter, the average final voltage output  $V_+$  reaches a higher level. The frequency converter circuit that uses  $V_+$  to control the clock period  $T$  is designed to reduce the power loss when the load is lighter.

The schematic of the frequency converter for TPMM is shown in Figure 4-1. In addition, the schematic of the frequency converter for MPVD is shown in Figure 4-2.

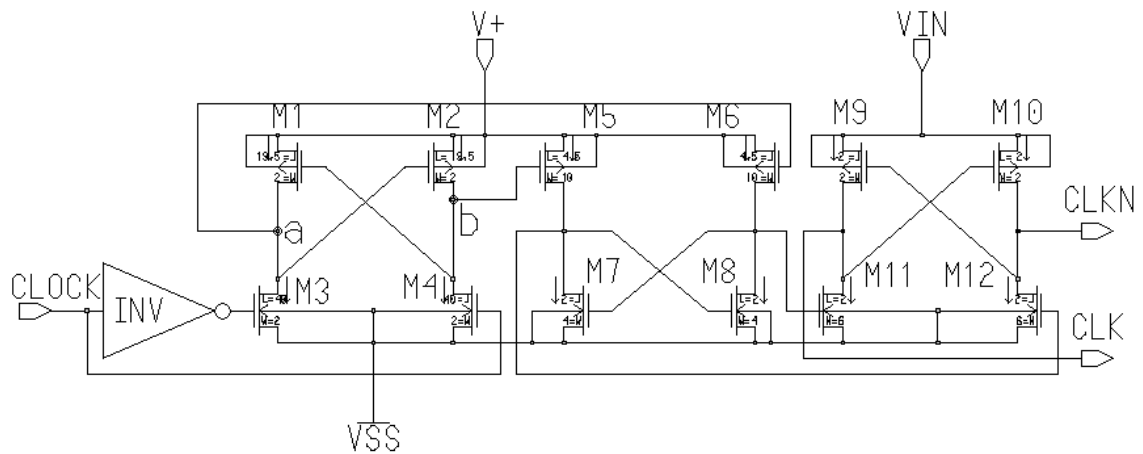


Figure 4-1: Frequency Converter for TPMM

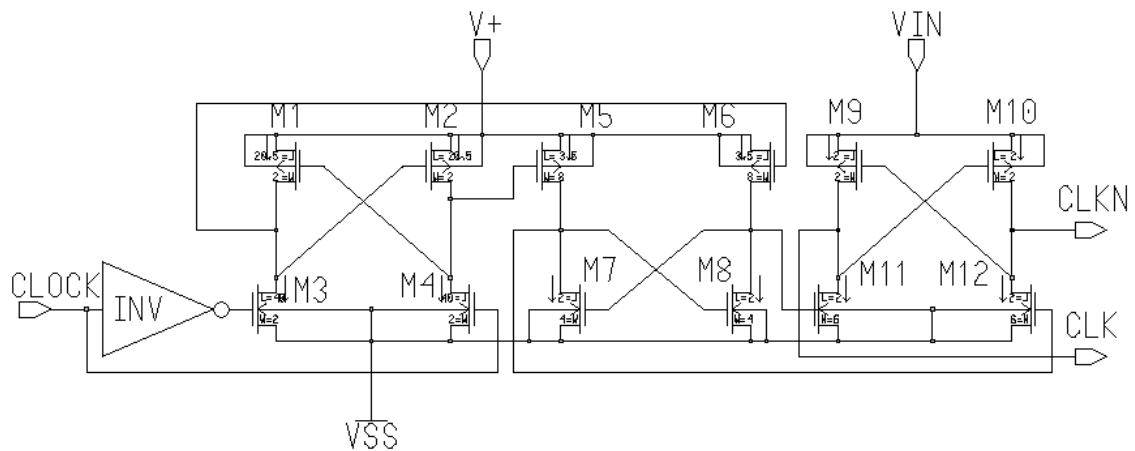


Figure 4-2: Frequency Converter for MPVD

These two circuits are very similar, except the ratios of W/L of the transistors are different. Their mechanisms are the same; for simplicity, we analyze Figure 4-1.

This circuit has 12 transistors, M1, M2 ... M12, CLOCK is the input, V+ the power supply, and CLKN and CLK are the outputs. The left part (left four transistors) is

the core of the circuit and it is used to convert frequency and shift the level of the clock to have amplitude of  $V_+$ . The middle part (middle four transistors) is designed to make the clock characteristic much sharper. The right part (right four transistors) is used to shift the level of the clock back to an amplitude of  $V_{IN}$ . This is because the output clock will be made non-overlapping -- it takes a lot more power using a clock with amplitude of  $V_+$  than with amplitude of  $V_{IN}$ .

## 4.2 Mechanism of Frequency Converters

Let us separate the left part from the whole circuit. Basically, this part has two stable states. When CLOCK is high, M1, M4 are turned on and M2, M3 are turned off. With the voltage  $V_a$  on node a equal to  $V_+$  and the voltage  $V_b$  on node b equal to 0, we define this state as State I. When CLOCK is low,  $V_a = 0$  and  $V_b = V_+$ , this state is defined as State II. At either stable state, there is no static current going through  $V_+$  to VSS for this part. We define the time taken from one state changing to the other after CLOCK change as the response time. If half of the clock period  $T$  of CLOCK is longer than the response time, the circuit is varying between these two static states. Otherwise, the circuit has no time to respond and will stay in one static state.

To analyze the response time for the circuit, let us first consider how the circuit changes from one state to another. Assuming the initial value of CLOCK is 3.3V and the initial state is state I ( $V_a = V_+$  and  $V_b = 0$ ). When CLOCK changes from 3.3V to 0V, at last the circuit will change to the other state ( $V_a = 0V$ , and  $V_b = V_+$ ). The change procedure is as follows

- Step 1>**, M3 is turned on and M4 is turned off.
- Step 2>**, With both M2 and M4 turned off, Vb keeps the previous value 0. With both M1 and M3 turned on, there is a current across V+ to VSS through M1 and M3. Va changes from V+ to a lower voltage.
- Step 3>**, When Va decreases enough to turn on M2, Vb changes from zero to a higher level.
- Step 4>**, When Vb changes to a voltage high enough to turn off M1, since M3 is on, Va arrives at 0V and the circuit goes to State II.

In Step 2, if the Va is a little lower than the  $V+ - V_{Tp}$ , it makes M2 in the edge of triode and cut-off state, the current through the M2 will be very small. In Step 3, since the gates of M1, M5 and the drain of M4 are connected to node b, to make Vb change from zero to a higher level, it costs time, and it is the main part of the response time.

To make Va a little lower than the  $(V+) + V_{Tp}$  in Step 2, M1 should work in triode state and M3 in saturation state. The equivalent circuit for the Step3 is shown in Figure 4-3, We use R1 and R3 to represent the turned-on resistors for M1 and M3. M4 is cut-off, M2 is in the edge of cut-off and saturation state, and R2 is the resistor for M2. To charge node b from 0V to V+,  $i_1$  has to charge the gate capacitors of M1 and M5 and the drain-bulk capacitor of M4. We use Cg1, Cg5, and Cd4 to represent these capacitors. The current  $i_1$  goes through M1 and M3 from V+ to VSS and is given as

$$\begin{aligned}
 i_1 &= m_p C_{ox} \frac{W_1}{L_1} \left\{ [(V+) + V_{Tp}] \times [(V+) - Va] - \frac{[(V+) - Va]^2}{2} \right\} \\
 &= m_n C_{ox} \frac{W_3}{L_3} (VIN - V_{Tn})^2
 \end{aligned} \tag{4-1}$$

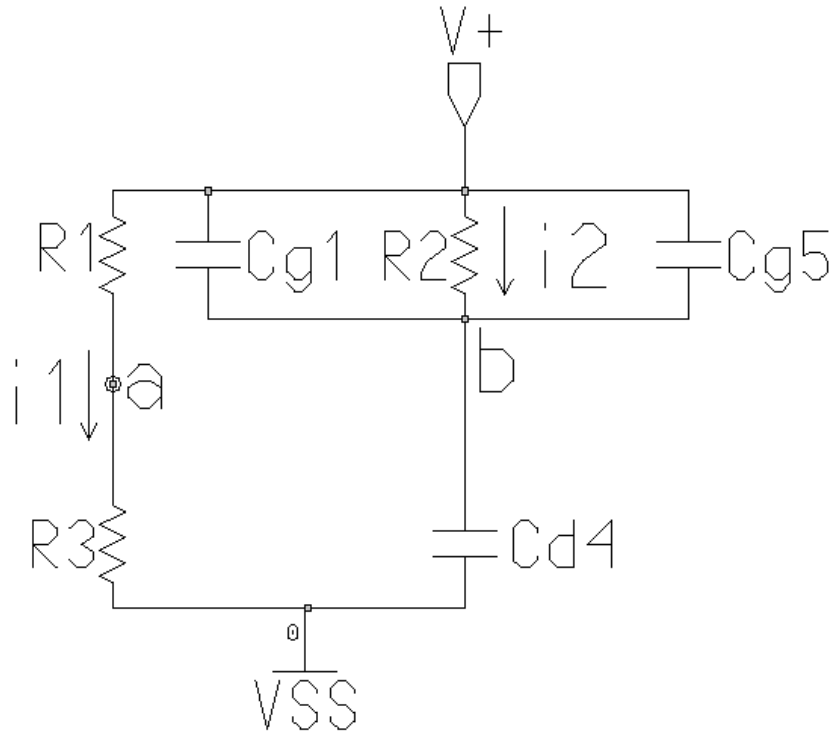


Figure 4-3: Equivalent Circuit of the Left Part of the Frequency Converter

For simplicity of analysis, let us neglect the modulation of M2 and M3 and the item  $[(V+) - Va]^2 / 2$ . We can get

$$Va = (V+) - \frac{m_n W_3 L_1 (VIN - V_{Tn})^2}{m_p W_1 L_3 [(V+) + V_{Tp}]} \quad (4-2)$$

In step 3, when M2 starts to be turned on, it works in triode state and Vb starts at 0V. The current  $i_2$  going through M2 from V+ to charge the gates of M1 and M5 is given by

$$i_2 = m_p C_{ox} \frac{W_2}{L_2} \left\{ [(V+) - Va + V_{Tp}] \times (V+) - \frac{(V+)^2}{2} \right\} \quad (4-3)$$

In Step 3,  $i_2$  is used to charge node b from 0V to V+, and the charge can be roughly estimated as

$$Q = (Cg1 + Cg5 + Cd4) \times (V+) \quad (4-4)$$

Since  $V+ \gg V_{Tp}$ , by ignoring the  $V_{Tp}$  item in equation (4-3), when  $V+$  increases, the current  $i2$  decreases, and the charge  $Q$  needed by changing node  $b$  increases due to the equation (4-4). It is obvious that to arrive at the conclusion, a higher  $V+$  results in a longer response time.

Let us assume that in Step 2 before the  $V_b$  is charged to  $(V+) + V_{Tp}$  (voltage for turning off the M1) the CLOCK changes back to 3.3V. M3 is turned off, then  $V_a$  will be  $V+$ , and the circuit stays in State I.

Let us select the suitable values of the  $W$  and  $L$  of the transistors to make the response time equal to half the clock period  $T/2$  (when  $V+$  equals the expected value),

When  $V+$  is higher than the expected value, it makes the response time shorter than  $T/2$ , the clock signal changes before the frequency converter enters the new steady-state, and the output clock stays in the previous state. Without the control signal changing, as the charge delivered to the load is lost in the circuit,  $V+$  will go down, and at last it will be less than the expected value. It makes the response time less than  $T/2$ ; the output clock will change with some delay, so the frequency has been regulated to lower and the output voltage is kept steady.

### 4.3 Simulation Results of the Frequency Converters

The W/L ratios of the transistors are chosen, as shown in Figure 4-1. When  $V_+$  is 15.5V, the response time of the frequency converter equals to the half clock period or 25 $\mu$ s.

Figure 4-4 shows that the simulation trace of the frequency converter,  $V_+$  is forced to change from 15V to 16V and then back to 15V, and CLOCK has the  $T = 50\mu$ s with amplitude 3.3V. When  $V_+$  is less than 15.5V, the response time for the converter to change from one steady-state to another is less than 25 $\mu$ s; i.e., the output clock CKO and CKON has the delay less than 25 $\mu$ s with the same period  $T = 50\mu$ s as the input clock. When the  $V_+$  is larger than 15.5V and the response time is larger than  $T/2$ , then the output stays in one steady-state without changing. When  $V_+$  goes down to 15.5V, the response time is reduced to less than  $T/2$  and the output clock restarts to change.

Similar to the TPVD frequency converter, the simulation result for MPVD frequency converter is shown in Figure 4-5. When  $V_+$  equals to 12.5V, the response time equals to  $T/2$ ; thus it can be used to achieve a steady voltage at 12.5V or so.



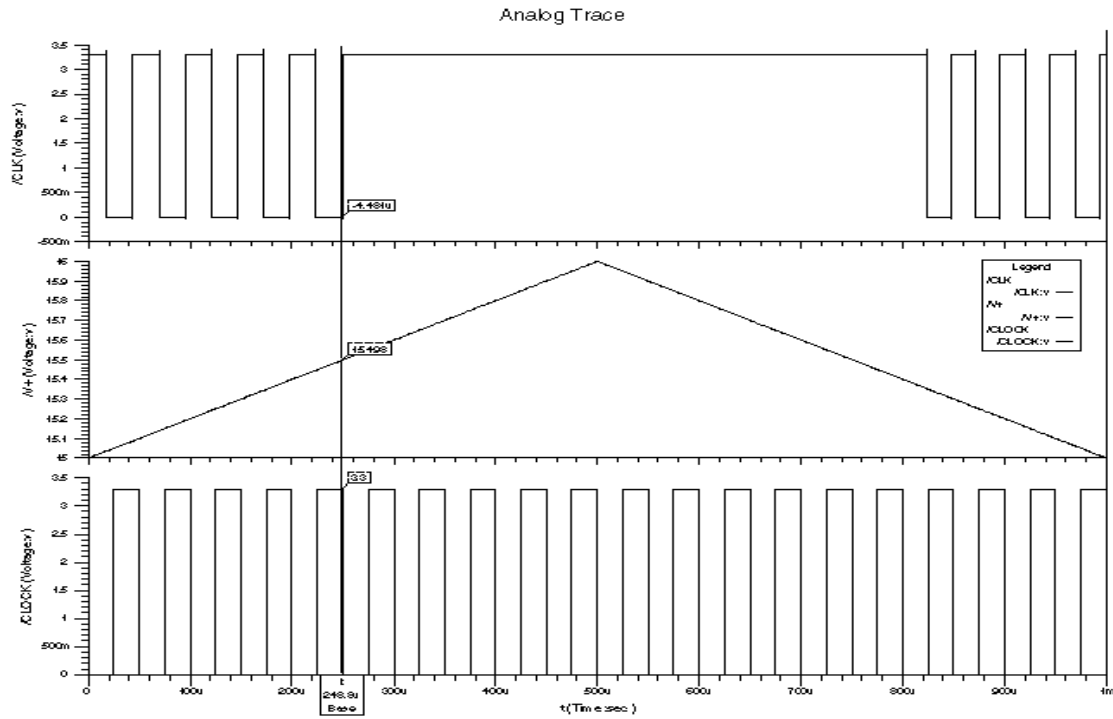


Figure 4-4: Simulation Result of TPMM Frequency Converter

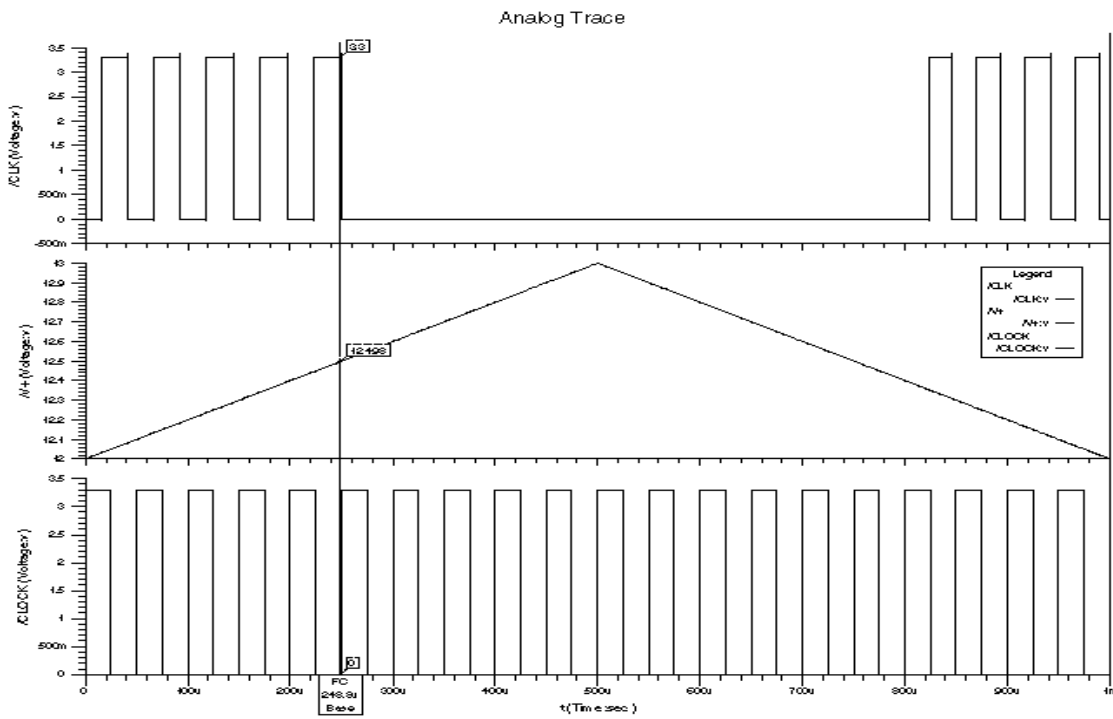


Figure 4-5: Simulation Result of MPVD Frequency Converter

## Chapter 5

### IMPLEMENTATION AND SIMULATION RESULTS

#### 5.1 Frequency Regulator

Chapter 4 introduced the frequency converters for TPMM and MPVD. These frequency converters are used to lower the switching frequency when the load becomes light and improve the power efficiency. For comparing the difference between the charge pump using frequency converter and that not using frequency converter, the frequency regulators are designed to enable or disable frequency conversion. The frequency regulators for TPMM and MPVD have the same structure except for using different frequency converters. The schematic of the frequency regulator for TPMM is shown in Figure 5-1.

The main part of the frequency regulator is the frequency converter, which is introduced in Chapter 4 -- the interior signals CLK and CLKN have a lower frequency than CLOCK when  $V_+$  is larger than 15.5V. There are 7 NAND2 gates and 2 inverters used to make output clock converted or not. When input FC\_EN is connected to VIN (3.3V), CLKO and CLKON have the same clock period as CLK and CLKN; their frequency is converted due to  $V_+$ . When we force FC\_EN to have 0V, CLKO and CLKON have the same period as CLOCK. The changes of the interior signals CLK and CLKN have nothing to do with the output clock; thus, the frequency converter is

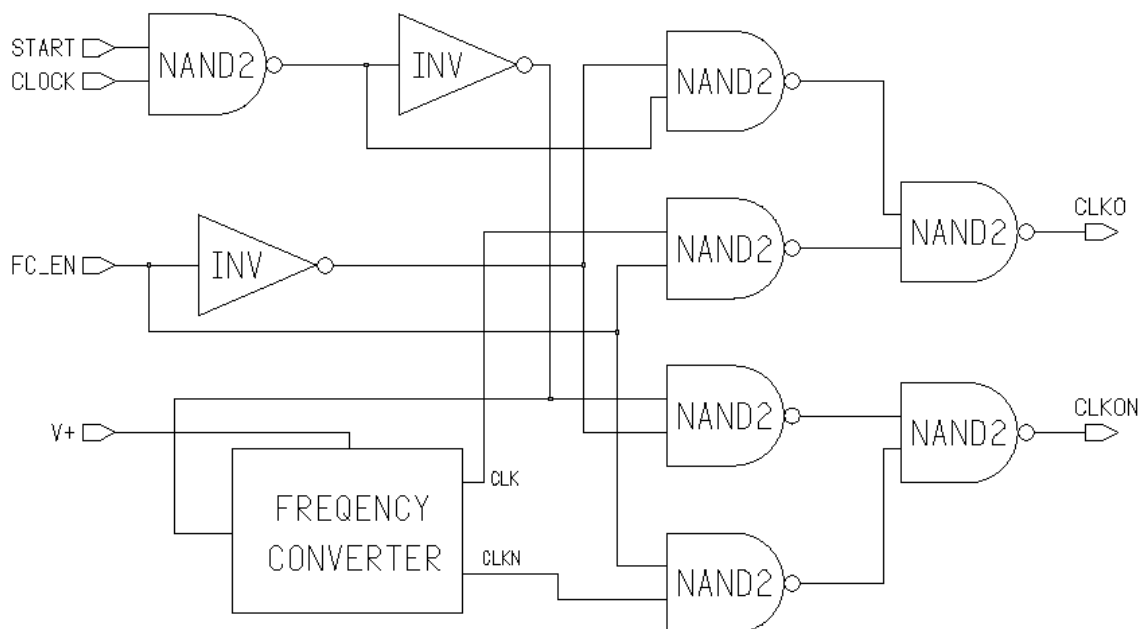


Figure 5-1: Diagram of Frequency Regulator

shielded. Input START controls the process of the charging. When it is 3.3V, the two-stage TPMM starts to charge; when it is 0V, TPMM stops switching.

## 5.2 Two-Stage TPMM with Frequency Regulator

Figure 2-1 shows the basic diagram of a two-stage TPMM. By inserting the frequency regulator between the input CLOCK and non-overlapping clock pair generator, we can get the two-stage TPMM with frequency regulator. The switching circuit and clock pair generator are implemented in the Orbit 2.0 $\mu\text{m}$  analog CMOS technology following the MOSIS SCMOS layout rules(see Appendix A). The layout is achieved using IC station (Mentor Graphics tool), and is shown in Appendix B. The die size is 2220 $\mu\text{m}$  \* 2250 $\mu\text{m}$  (standard size of tiny chips for educational use). We can see that the ten large transistors occupy more than half the area. Because of the limitation of the

wafer's size, the diode and the four capacitors are implemented using separate components.

### 5.2.1 Implementation of TPMM

To implement this TPMM into the tiny chip, a new layout frame is designed. The standard frame provided by MOSIS fabrication services has two voltage rings around the tiny chip; they are prepared for the power supply and the ground. Since  $V_+$  is used to give back higher voltage for driving buffers, frequency converter, and all of the substrates of PMOS, a wire ring for  $V_+$  is added to the new frame around the tiny chip. Using these three wire rings, the connection of the layout is much easier and the length of the wires is much shorter than that if no rings are used. Every pin of the designed frame has the exact layer, size and position as the standard frame, and the frame meets all the rules of SCNA Orbit 2.0 $\mu\text{m}$  provided by the MOSIS fabrication services.

The comb structure is used for the large transistors. Since  $W$ 's value of PMOS is 6000 $\mu\text{m}$  and that of NMOS is 3000 $\mu\text{m}$ , both of them are longer than the die's size, and we cannot let the polysilicon of gate be straight in the tiny chip. The  $W$  of PMOS is divided into 60 sections of 100 $\mu\text{m}$  each, while that of NMOS is divided into 30 sections. This divided polysilicon share the drains and sources with each other, and the area of the transistors is dramatically reduced. By using this structure, the sizes of the transistor drain and source are much less than that of straight polysilicon. As discussed in Chapter 2, the bulk-source and bulk-drain of the transistors depend on the perimeter of the transistors; hence, this structure can reduce the value of the bulk-source (drain) capacitors and, thus

reduce the dynamic power loss during switching. This is another advantage of using the comb structure. For the same reasons, the driving buffers are also designed to have the comb structure to save the area and improve design efficiency.

To avoid the transmission of the large current, four pins are used for VIN, five pins for VSS, and three pins for V+. The metal wire (metal 1 layer) connecting these four large capacitors are selected to have a width of 100 $\mu\text{m}$ , which is as large as possible for this tiny chip. According to the perimeter provided by MOSIS, the maximum current density for the metal 1 layer is 68 $\mu\text{A}/\mu\text{m}$ , which means that the maximum current to go through the charge pump is 6.8mA. As analyzed before, the current through these large transistors depends on the load; when the load resistor becomes large, the current is smaller. The limitation of the current limits the load and, thus, limits the driving ability for this charge pump.

The layout of TPMM in appendix B shows that there are three buffers in the wire of the input signal CLOCK, START, and FC\_EN. They are used to prevent the charge pump from being disturbed by the outside environment.

### **5.2.2 Simulation Result of TPMM**

After I got the layout of 2-stage TPMM, I used the IC station to get the parasitic extraction for this charge pump, and then I simulated this charge pump under different load resistor conditions. A SPICE model file (Appendix C is used for the Accusim II (Mentor Graphics tool)).

First, I simulated the charge pump without frequency conversion under no load condition by selecting the input START to be 3.3V at 1 $\mu$ s (initial value is 0V), and setting FC\_EN to be 0V to prevent the switching frequency from being converted. Figure 5-2 shows the simulation results of V+ under no-load; V+ has the initial value at 2.6V or so because the diode is connected between the power source and V+. V+ grows quickly in the beginning of charging, then it increases gradually, and after 15ms (300 clock periods) the output voltage reaches 16.482V and it is 4.9945 times as large as the power supply 3.3V. In Equation 2-9, when RL is infinite the output voltage V+ is 5\*VIN. This simulation result matches Equation 2-9 very well.

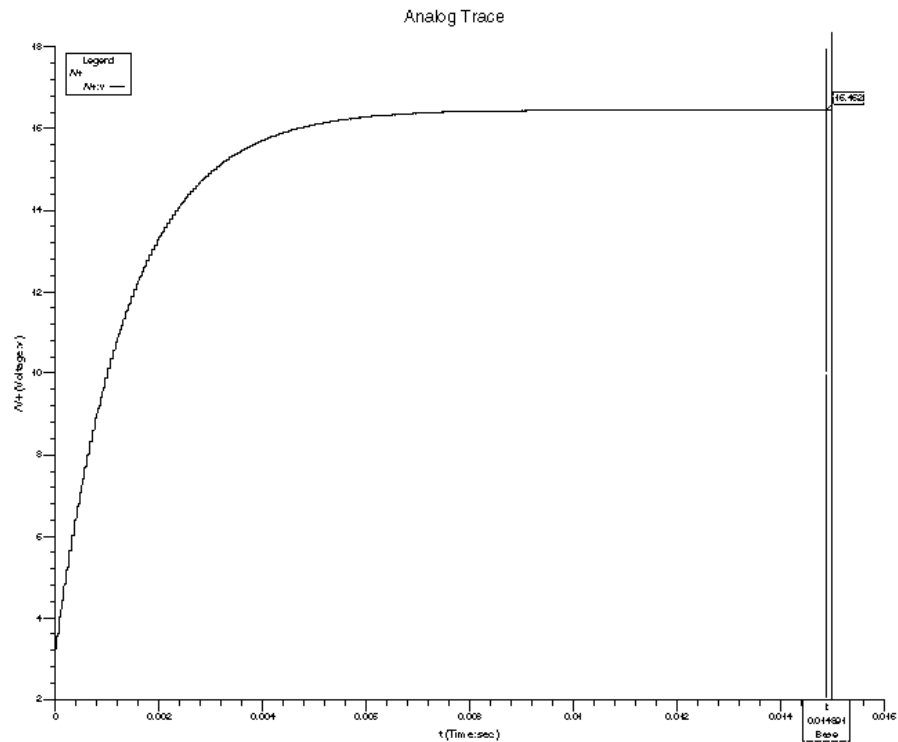


Figure 5-2: V+ of TPMM without Frequency Conversion

By forcing FC\_EN to have 3.3V to let the switching frequency be converted by the feedback of V+, the results of V+ for the two-stage TPMM with frequency converting is shown in Figure 5-3. In the beginning of the process, the results have the same characteristics as those in Figure 5-2. After 3.8ms (76 clock periods), the output voltage reaches 15.5V; this value of V+ makes the switching clock converted to a lower level. The simulation results reveal that the period of the switching frequency is converted from 20kHz to about 100Hz. V+ stays at 15.5V with a deviation of  $\pm 0.15V$ . This charge pump works at low frequency to make up the power loss during switching and keeps the output voltage at a high level.

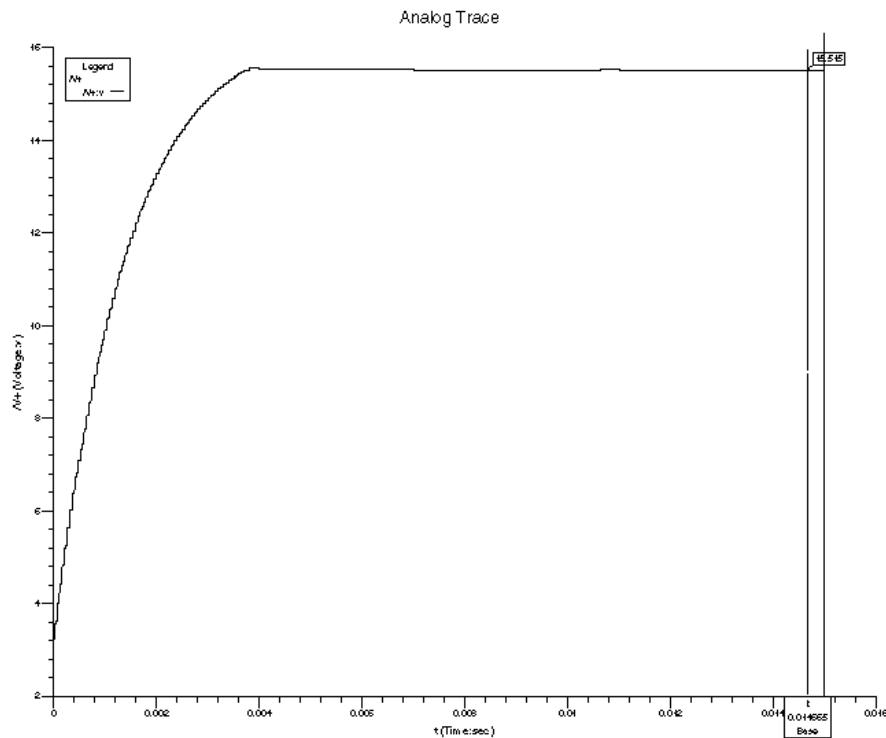


Figure 5-3: V+ of TPMM with Frequency Conversion

By adding the different load resistor  $R_L$  to this charge pump, I arrived at simulation results for the two-stage MPVD with different  $R_L$ , as shown in Table 5-1.  $P_{in}$  represents the average power supplied by  $V_{IN}$  and  $P_{out}$  the average power consumed in  $R_L$ . Since the initial value for the  $V_+$  is very low compared to the final value, the voltages on the capacitors in the beginning are much lower than those at the end. The growth of the voltages on the capacitors needs energy from the power supply, after 300 clock periods,  $V_+$  goes to its final value and the voltages on the capacitors stay at the steady level. The charge pump goes to its steady state that the power provided by  $V_{IN}$  is used to support the output power and make up the power loss in the circuit.  $P_{in}$  and  $P_{out}$  in Table 5-1 are calculated using the time period between 15ms and 20ms (during 300 clock periods to 400 clock periods). The power efficiency is calculated by the ratio of the average input power over the average output power.

Table 5-1: Simulation Results of  $V_+$  and Power Efficiency for TPMM

RL(Ohm)	TPMM without frequency regulation				TPMM with frequency regulation			
	V+ (V)	Pin(mW)	Pout(mW)	Efficiency(%)	V+ (V)	Pin(mW)	Pout(mW)	Efficiency (%)
no load	16.48	3.02	0	0	15.49	0.153	0	0
100K	16.42	5.88	2.71	46.1	15.49	2.94	2.41	82.0
50K	16.37	8.83	5.38	60.9	15.49	5.97	4.84	81.1
20K	15.92	16.4	12.7	77.4	15.49	13.9	12.2	87.8
10K	15.14	28.8	23.0	79.9	15.14	28.9	23.1	79.9
5K	14.15	48.9	40.2	82.2	14.15	49.1	40.2	81.9
2K	12.87	117	83.7	71.5	12.87	117	83.7	71.5
1K	10.11	211	106	50.0	10.11	211	106	50.0
500	7.13	334	104	31.1	7.13	334	104	31.1



The left sections of Table 5-1 shows the results without frequency conversion.  $V_+$  goes down with the decrease of load resistor  $R_L$ . It reaches its highest value when there is no load, and  $V_+$  can only reach 7.13V when  $R_L$  is  $500\Omega$ . Equation 2-9 gives us the relationship of the average  $V_+$  and  $R_L$  under the ideal conditions of two-stage TPMM -- smaller  $R_L$  results in lower  $V_+$ .

Let us compare these two results. They have the same features, but the simulation value of  $V_+$  goes down much faster than the results calculated from Equation 2-9 due to the power loss in the circuit. When the load is about  $1K\Omega$ , the power output driving ability is at its maximum value of 106mW. These values are far from the values calculated from Equations 2-11 and 2-12, but also reveal that there exists an optimum value for  $R_L$  to get the maximum value for the output power. When the TPMM has its highest output power, the power efficiency is only 50.0%. This huge power loss can harm the integrated circuit during switching. The maximum power efficiency (81.9%) occurs when the load resistor is  $5K\Omega$ ; where the TPMM works at a heavier or lighter load than  $5K\Omega$ , the power efficiency is lower.

The right section of Table 5-1 shows the results with frequency conversion. When the load resistor is no more than  $5k\Omega$ , the results are almost identical to those of the left section. This means the frequency converter does not affect the circuit's performance because the  $V_+$  is not high enough to convert the controlling clocks. When the load becomes light, the output voltage stays at 15.49V, resulting in the power output being a little lower than that of the upper part. Nevertheless, the power efficiency is dramatically improved. When there is no load, even the power efficiency is 0% but the input power is

only 0.153mW, while without a frequency regulator it is 3.02mW. This reduces the power loss by a factor of 20 or so. When the load resistor  $R_L$  is no less than 5K, the power efficiency of this charge pump can have power efficiency about higher than 80%. We can also see from Table 5-1 that a steady average voltage output of 15.49V is obtained when the  $R_L$  is no less than 20k $\Omega$ . A stable level of the output voltage with different load values is another advantage of the frequency regulation used.

### **5.3 Two-Stage MPVD with Frequency Regulator**

The layout of 2-stage MPVD is shown in Figure in Appendix B, which is similar to the TPMM. After extracting the parasitic from the layout, I also got the Back-Annotated simulation results. Figure 5-4 shows the simulation results of  $V_+$  under no load without frequency regulation. After 10ms (200 clock periods), the output voltage reaches 13.182V and is 3.995 times as large as the power supply 3.3V; it matches Equation 3-11 which gives the voltage gain of 4. Figure 5-5 displays  $V_+$  with frequency regulation when no-load. After 3.65ms (73 clock periods), the output voltage reaches 12.5V, then stays at this level with a deviation of  $\pm 0.11V$ . The period of the controlling clock pair CK1 and CK2 is converted from 20kHz to 80Hz or so, and CK3 and CK4 work at about 40Hz.

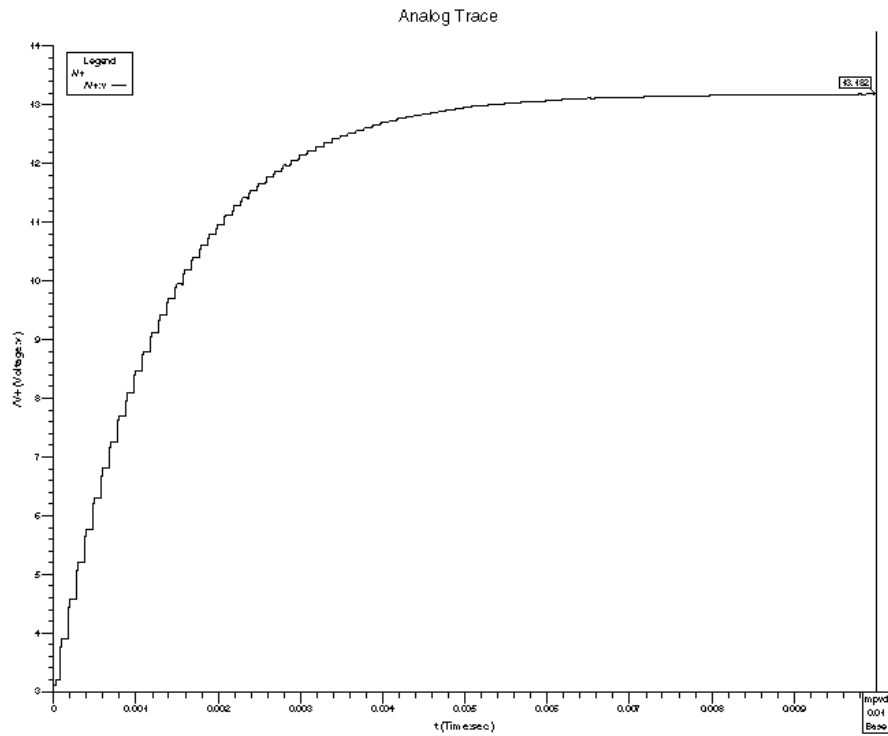


Figure 5-4: V+ of MPVD without Frequency Conversion

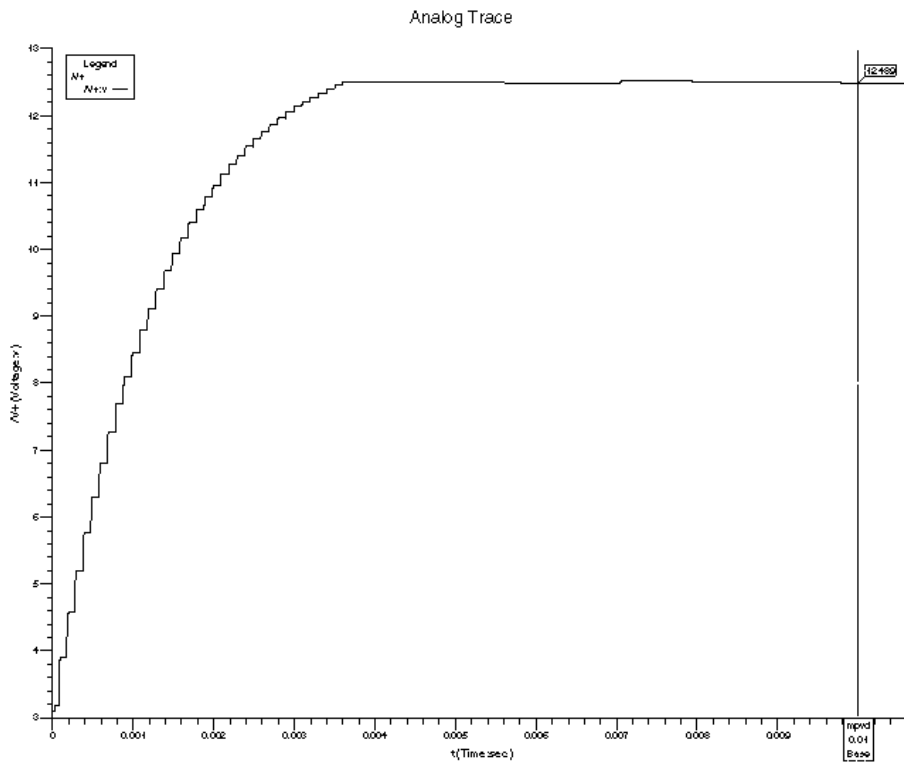


Figure 5-5: V+ of MPVD with Frequency Conversion

Table 5-2 shows the simulation results of the two-stage MPVD with different load resistors. The left part shows the results without frequency converting, in which the  $V_+$  goes down with the decreasing load resistors, and when the load  $R_L$  is  $500\Omega$ , the output voltage can only reach  $5.11V$ . When the load is about  $1K\Omega$ , the power output voltage can only reach  $5.11V$ . When the load is about  $1K\Omega$ , the power output driving ability is at its maximum value of  $56.2mW$ , but the power efficiency is only  $41.9\%$ . The maximum power efficiency ( $84.6\%$ ) occurs when  $R_L$  is  $5K\Omega$ . The right parts of Table 5-1 show the results with frequency converting. When  $R_L$  is no more than  $5k\Omega$ , the simulation results of the right section is almost the same as those of the left section. When the load becomes light, the output voltage stays at  $12.50V$ , and the power efficiency is dramatically improved. When there is no load, the input power is  $0.083mW$ , while without a frequency regulator it is  $1.85mW$ . This reduces the power loss by a factor of 22. A steady voltage output of  $12.5V$  is obtained when the  $R_L$  is no less than  $5k\Omega$ .

Table 5-2: Simulation Results of  $V_+$  and Power Efficiency for MPVD

RL(Ohm)	MPVD without frequency regulation				MPVD with frequency regulation			
	V+ (V)	Pin(mW)	Pout(mW)	Efficiency(%)	V+ (V)	Pin(mW)	Pout(mW)	Efficiency (%)
no load	13.18	1.85	0	0	12.5	0.083	0	0
100K	13.16	3.85	1.73	44.9	12.5	1.75	1.56	89.1
50K	13.11	5.32	3.44	64.7	12.5	3.43	3.13	91.3
20K	12.92	10.5	8.36	79.6	12.5	8.46	7.81	92.3
10K	12.55	18.9	15.8	83.6	12.5	17.2	15.6	90.7
5K	11.87	33.7	28.5	84.6	11.87	33.7	28.3	84.0
2K	9.75	73.2	47.9	65.4	9.75	73.5	47.6	64.8
1K	7.46	134	56.2	41.9	7.46	134	56.1	41.9
500	5.11	255	53.3	20.9	5.11	255	53.3	20.9

## Chapter 6

### TEST REPORT AND CONCLUSION

#### 6.1 Test Report

This test report was based on the test of the sample chips fabricated by MOSIS. The simulation results presented in Chapter 5 were satisfactory, they agreed with the basic concept of the proposed structures, and the power efficiencies were also very high when the load resistances were in the proper range. After getting the layouts of the two charge pumps, I sent them out to MOSIS for fabrication. I received 8 sample chips 12 weeks later, four chips of MPVD and the other four of TPMM. I used measurement instruments from the store of Electrical Engineering Department. These instruments included a pulse generator, an oscilloscope, a DC power supply and a multi-meter. I also bought some components such as the resistors, diodes and capacitors. Then I built two test circuits for MPVD and TPMM separately. Since many parts of the charge pumps were integrated inside the chips, these test circuits were not very complicated.

Firstly I tested the MPVD, in the beginning, I used exactly the same conditions as that used for the simulation. By applying 3.3V as the power supply and no load in the output, the output voltage (V+) measured by the multi-meter was 3.3V. Because there was a diode connected between the power supply and the V+, it meant that the MPVD did not work at all. I tried to test it in many different conditions by changing the

frequency of the input CLOCK and putting the different resistors in the output, but the output  $V_+$  did not change at all. Then I replaced another MPVD sample chip, the same condition occurred. I had to think about it carefully, it was too early to conclude that these chips were wrongly designed or fabricated. Even though I did not see anything unusual by eye and I did not catch any signals with sharp glitch in the oscilloscope or the multi-meter, I supposed that the two tested chips were burnt when I turned on the switch of the power supply. There must be a transistor whose breakdown voltage was not large enough to afford the high voltage  $V_+$ . It seemed that I had to change the voltage of the power supply into a lower level. I applied the power at 1.0V and then pulled it higher gradually. At the beginning, the  $V_+$  kept the same value as the power supply. When the power supply arrived 2.1V,  $V_+$  jumped to about 8.2V. The MPVD sample chip worked and it could offer much higher voltage than the power supply. Since I had only two MPVD sample chips left, I decided to use 2.3V as the power supply to get the test report first, and then see if it is possible to use a higher voltage.

Table 6-1 shows the test results of the two-stage MPVD with different load resistors by using the 2.3V as the power supply. The values of the load resistors were measured by using the multi-meter. The frequency of the input clock is 20 kHz - the same as used in simulation. The load capacitor  $C_L$  is  $3.3\mu\text{F}$ , and the other capacitors are  $0.47\mu\text{F}$ .

Similar to the simulation results shown in Table 5-1, the tested  $V_+$  goes down with the load resistance's decreasing. When there is no load, the  $V_+$  can reach its highest value at 8.93V that is 3.883 times of the power supply (2.3V), and is lower than the corresponding simulation result (3.995 times) but is also close to the ideal (4 times).

When the load was  $4.84\text{k}\Omega$ , the MPVD sample chip got its highest power efficiency 81.4%, which is lower than that of the simulation result. The highest power efficiency of the simulation is 84.6% when the load is  $5\text{k}\Omega$ . Because the simulation tools regard the capacitors and the outside wires as the ideal, the tested power efficiency is lower according to the power loss in the outside circuit. When the load resistor is less than  $4.84\text{k}\Omega$ , the output power becomes higher but the power efficiency becomes lower, which are just like the simulation results.

Unfortunately the frequency regulator could not work at all. I tried many different conditions by changing the input frequency from 1kHz to 500kHz, but it did not regulate the work frequency or it changed the frequency too little to be measured. Since this frequency regulator was designed for the use in charge pump with the power supply 3.3V, it is very sensitive to the working voltage and could not work when applying 2.3V as the power supply.

Table 6-1: Test Results of MPVD

MPVD (VIN=2.3V)					
RL(Ohm)	V+ (V)	I (mA)	Pin(mW)	Pout(mW)	Efficiency(%)
no load	8.93	0.94	2.16	0	0
99k	8.87	1.21	2.79	0.79	28.3
48.5k	8.77	1.63	3.75	1.59	42.4
21.9k	8.56	2.21	5.08	3.35	65.9
9.96k	8.1	3.69	8.49	6.59	77.6
4.84k	7.29	5.86	13.48	10.98	81.5
2.18k	6.02	8.45	19.44	16.62	85.5
1.01k	4.42	13.05	30.02	19.34	64.4
509	3.06	14.65	33.7	18.4	54.6

Because the first two MPVD sample chips were burnt, I used 2.3V as the power supply of TPMM. Table 6-2 shows the test results of the two-stage TPMM with different load resistors. The CLOCK is 20KHz, the load capacitor CL is 3.3 $\mu$ F, and the other capacitors are 0.47 $\mu$ F.

When there is no load, the output voltage (V+) can reach 9.5V that is 4.13 times than the power supply (2.3V). When the load is 2.18K $\Omega$ , the power efficiency has its highest value 85.5%. The V+ goes down when the load becomes heavier. And the frequency regulator did not work for TPMM either.

Table 6-2: Test Results of TPMM

TPMM (VIN =2.3V)					
RL(Ohm)	V+ (V)	I (mA)	Pin(mW)	Pout(mW)	Efficiency(%)
no load	9.5	2.57	5.91	0	0
99k	9.48	2.59	5.96	0.91	15.3
48.5k	9.47	2.61	6.00	1.85	30.8
21.9k	9.41	2.95	6.79	4.04	59.5
9.96k	8.77	4.29	9.87	7.72	78.2
4.84k	7.89	6.87	15.80	12.86	81.4
2.18k	6.34	10.33	23.76	18.44	77.6
1.01k	4.93	15.25	35.08	24.06	68.6
509	3.21	14.97	34.43	20.24	58.8

To make sure why the first two MPVD sample chips did not work and figure out the highest power supply these charge pumps could work, I tried to use the higher power



supply on TPMM, started at 2.3V with no load, then made the power supply have higher value gradually. The  $V_+$  increased with the power supply's increasing, when the power supply reached 2.52V, the output voltage  $V_+$  had a value at 10.6V then suddenly went down to 2.52V. When I changed the power supply back to 2.3V, the  $V_+$  could not get the higher voltage than the power supply, so it was apparently burnt. To figure out where the problem was and which part was burnt, I tried to test the connections between pins of the sample chips by applying different power supplies and frequencies. But I could not figure it out due to the limitation of the number of the test pins.

If the limitation of the area of the tiny-chip were not so strict, at least two other parts should have been integrated to these charge pumps. The first one is the protection circuit for large current and high voltage, and the other one is the test circuit to make it easy to figure out the design and fabrication problems.

I took many photos of the test circuits and the waveforms shown in the oscilloscope, unfortunately, none of them are clear enough to be scanned to the appendix.

## **6.2 Conclusion**

Two charge pumps were designed, simulated and fabricated into integrated circuits. Both the simulation results and test results agree with the theoretical models. The concept of Starzyk charge pump (MPVD) has been verified by the test of the sample chips. And the main objective of this thesis has been accomplished.

Many things were done to make these charge pumps work properly. Firstly Dr. Starzyk taught me about the basic concept of MPVD and gave me a lot of advice, we also

analyzed and discussed several issues in detail, such as the driving ability, power efficiency and the highest voltage that could be achieved. Secondly I designed several additional circuits to implement the charge pumps by using CMOS process, such as the clock non-overlapping generators, voltage level shifters and frequency regulators circuits. Thirdly the layouts such as the pads, buffers, and the power and ground rings were made according to the MOSIS SCMOS layout rules. Finally, two test circuits were built to test these sample chips.

By using the Mentor Graphics simulation tools, the simulation results of the MPVD and TPMM agree with the theoretical models very well, and the power efficiencies of them were very satisfactory by using the frequency regulator. The sample chips could only work when the power supply was between 2.1V and 2.5V. Thus the frequency regulators do not work, and it causes the power efficiencies to be lower when the load becomes lighter. However, the test results of the sample chips also agree with the theoretical models very well.

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## Appendix A

### MOSIS SCMOS LAYOUT RULES

MOSIS is a small-volume production service for VLSI circuit development. To implement the TPMM and MPVD into the SCNA Orbit 2.0 $\mu$ m analog SCMOS technology, I used IC Station and followed exactly the SCMOS layout rules provided by MOSIS. The following is the SCMOS layout rules for different layers.

Rule code	SCMOS Layout Rules - Well	$\lambda$ (1.0 $\mu$ m)
1.1	Minimum width	10
1.2	Minimum spacing between wells at different potential	9
1.3	Minimum spacing between wells at same potential	0 or 6
1.4	Minimum spacing between wells of different type	0
	SCMOS Layout Rules - Active	
2.1	Minimum width	3
2.2	Minimum spacing	3
2.3	Source/drain active to well edge	5
2.4	Substrate/well contact active to well edge	3
2.5	Minimum spacing between active of different implant	0 or 4

SCMOS Layout Rules - Select		
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3
4.2	Minimum select overlap of active	2
4.3	Minimum select overlap of contact	1
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must not overlap) (not illustrated)	2
SCMOS Layout Rules - Poly		
3.1	Minimum width	2
3.2	Minimum spacing	2
3.3	Minimum gate extension of active	2
3.4	Minimum active extension of poly	3
3.5	Minimum field poly to active	1
SCMOS Layout Rules - Simple Contact to Poly		
5.1	Exact contact size	2 x 2
5.2	Minimum poly overlap	1.5
5.3	Minimum contact spacing	2
5.4	Minimum spacing to gate of transistor	2
SCMOS Layout Rules - Simple Contact to Active		

6.1	Exact contact size	2 x 2
6.2	Minimum active overlap	1.5
6.3	Minimum contact spacing	2
6.4	Minimum spacing to gate of transistor	2
	SCMOS Layout Rules - Pbase (Analog Option)	
16.1	All active contact	2 x 2
16.2	Minimum emitter select overlap of contact	3
16.3	Minimum pbase overlap of emitter select	2
16.4	Minimum spacing between emitter select and base select	4
16.5	Minimum pbase overlap of base select	2
16.6	Minimum base select overlap of contact	2
16.7	Minimum nwell overlap of pbase	6
16.8	Minimum spacing between pbase and collector active	4
16.9	Minimum collector active overlap of contact	2
16.10	Minimum nwell overlap of collector active	3
16.11	Minimum select overlap of collector active	2
	SCMOS Layout Rules - Buried Channel CCD (2um Analog Option)	



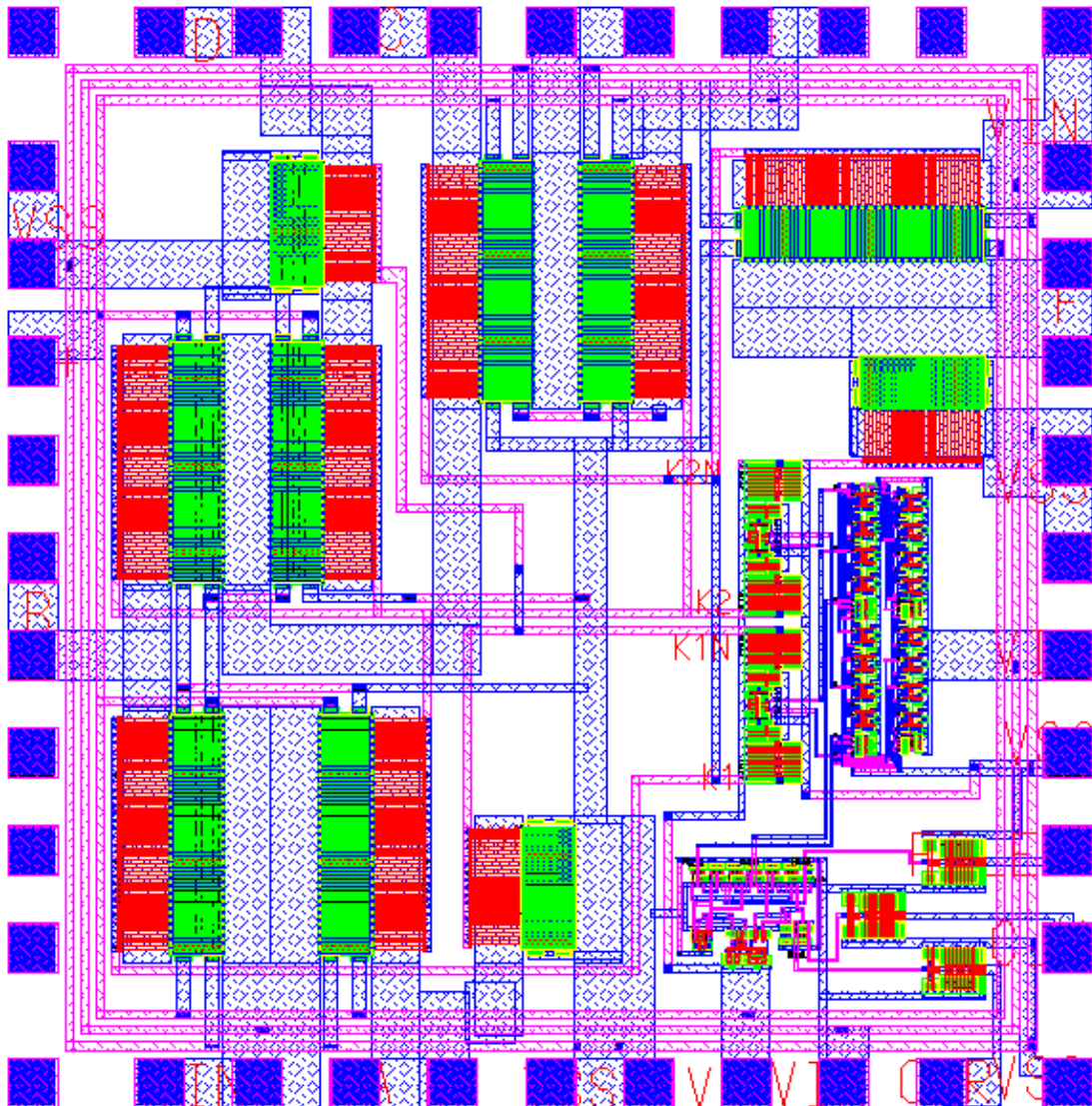
19.1	Minimum CCD channel active width	4
19.2	Minimum CCD channel active spacing	4
19.3	Minimum CCD implant overlap of channel active	2
19.4	Minimum outside contact to CCD implant	3
19.5	Minimum select overlap of electrode (or poly)	2
19.6	Minimum poly/electrode overlap within channel active	2
19.7	Minimum contact to channel electrode (or poly)	2
SCMOS Layout Rules - Metall		
7.1	Minimum width	3
7.2.a	Minimum spacing	3
7.2.b	Minimum tight metal spacing (only allowed between minimum width wires - otherwise, use regular spacing rule)	2
7.3	Minimum overlap of any contact	1
SCMOS Layout Rules - Via1		
8.1	Exact size	2 x 2
8.2	Minimum via1 spacing	3
8.3	Minimum overlap by metall	1
8.4	Minimum spacing to contact	2

8.5	Minimum spacing to poly or active edge	2
SCMOS Layout Rules - Metal2		
9.1	Minimum width	3
9.2.a	Minimum spacing	4
9.2.b	Minimum tight metal or SUBM spacing (only allowed between minimum width wires - otherwise, use regular spacing rule)	3
9.3	Minimum overlap of via1	1
SCMOS Layout Rules - Overglass		
10.1	Minimum bonding pad width	100 x 100
10.2	Minimum probe pad width	75 x 75
10.3	Pad metal overlap of glass opening	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to unrelated active, poly or poly2	15

## Appendix B

### LAYOUTS OF THE CHARGE PUMPS

#### B.1 Layout of the 2-Stage TPMM





## Appendix C

### SCNA ORBIT 2.0mM SPICE MODEL FILE

To get the correct simulation results for TPMM and MPVD, a SPICE model file provided by MOSIS is used for the analog simulator Accusim II (Mentor Graphics tool).

The SPICE models for PMOS and NMOS are shown as follows:

```
.MODEL CMOSN NMOS LEVEL=2 PHI=0.700000 TOX=3.9900E-08 XJ=0.200000U
+ TPG=1 VTO=0.7843 DELTA=2.4530E+00 LD=1.8020E-07 KP=6.7219E-05
+ UO=776.7 UEXP=1.1460E-01 UCRIT=6.9380E+03 RSH=1.8300E+01
+ GAMMA=0.5907 NSUB=7.8720E+15 NFS=9.0900E+10 VMAX=5.4300E+04
+ LAMBDA=3.5030E-02 CGDO=2.3393E-10 CGSO=2.3393E-10
+ CGBO=3.4582E-10 CJ=1.2836E-04 MJ=6.9765E-01 CJSW=5.6429E-10
+ MJSW=2.5604E-01 PB=4.2345E-01

.MODEL CMOSP PMOS LEVEL=2 PHI=0.700000 TOX=3.9900E-08 XJ=0.200000U
+ TPG=-1 VTO=-0.9729 DELTA=1.9930E+00 LD=2.2310E-07 KP=1.8079E-05
+ UO=208.9 UEXP=3.0810E-01 UCRIT=1.0540E+05 RSH=3.7600E+01
+ GAMMA=0.7449 NSUB=1.2520E+16 NFS=7.1500E+11 VMAX=9.3560E+05
+ LAMBDA=5.0490E-02 CGDO=2.8962E-10 CGSO=2.8962E-10
+ CGBO=3.4582E-10 CJ=3.2805E-04 MJ=6.1671E-01 CJSW=3.7972E-10
+ MJSW=1.9983E-01 PB=9.0000E-01
```

## Appendix D

### GLOSSARY OF SYMBOLS

$C_1, C_2 \dots C_n$	Transferring capacitors
$C_{gs}$	Gate-source overlap capacitance
CL	Load capacitor
$f_P$	Power efficiency (%)
L	Length of the transistors' poly
M1, M2 ... M10	Large transistors used as switches
$P_{D/S}$	Dynamic power loss of the drain/source
$P_g$	Dynamic power loss of the gate
Pin	Input power of the charge pumps
Pout	output power of the charge pumps
$P_R$	Resistive power loss
RL	Load resistor
T	Input clock period
UO	Electron mobility
VIN	Power supply (source)
VT	Zero-bias threshold voltage
V+	Voltage output
W	width of the transistors' poly