ANALOG AND MIXED-SIGNAL

TEST AND FAULT DIAGNOSIS

A Dissertation Presented to

The Faculty of the

Fritz J. and Dolores H. Russ
College of Engineering and Technology

Ohio University

In Partial Fulfillment

of the Requirements for the Degree

Doctor of Philosophy

by

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August, 2003

THIS DISSERTATION ENTITLED

"ANALOG AND MIXED-SIGNAL TEST AND FAULT DIAGNOSIS"

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ACKNOWLEDGEMENTS

I want to thank all the persons who help me finishing this dissertation. Although I cannot list them all within this small page, I do want to express my deepest gratitude to some of them directly involved in my Ph. D research.

I would like to sincerely thank my advisor, Prof. Janusz A. Starzyk, for his guidance, support and encouragement. His insight and knowledge in analog testing were the greatest benefits to this dissertation work.

Many sincere thanks are due to my dissertation committee members, Prof. Robert A. Curtis, Prof. Herman W. Hill, Prof. Henryk J. Lozykowski and Prof. Sergiu Aizicovici, for their time, instructions, and patience during my dissertation research.

I am also greatly thankful to Mr. Genard N. Stenbakken for his instructions when I was working at NIST. This dissertation could not be finished without his knowledge, skill, and support.

I am pleased to acknowledge the financial support from NIST and Stocker Research Associateship at College of Engineering, Ohio University during my research work.

Finally, special thanks to my wife, Ying, and my parents, for their support and encouragement all of these years.

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LIST OF ABBREVIATIONS

ADC	Analog-Digital-Converter
AI	Artificial Intelligence
ATE	Automated Test Equipment
BIST	Built-in-Self-Test
CDF	Cumulative Density Function
CSL	Cumulative-Sum-Limited
CUT	Circuit-Under-Test
DAC	Digital-Analog-Converter
DC	Direct Current
DFT	Design-for-Testability
GPS	Global Positioning System
IC	Integration Circuit
ICDF	Inverse Cumulative Density Function
IT	Information Technology
KCL	Kirchhoff Current Law
NIST	National Institute of Standards and Technology
PDF	Probability Density Function
PLL	Phase-Locked-Loop
RF	Radio Frequency
PME	Phase-Maximum-Error
RMS	Root-Mean-Square
S&H	Sample & Hold
SAT	Simulation-After-Test
SBT	Simulation-Before-Test
SoC	System-on-Chip
TTM	Time-to-Market

TTV	Time-to-Volume
VLSI	Very Large Scale Integration circuits

CHAPTER 1 INTRODUCTION

Analog and mixed-signal test and fault diagnosis play an essential role in circuit design, device production, and instrumentation maintenance. It is the most challenging area in electronics test for academic researchers and industrial engineers [1-4]. The purpose of test and fault diagnosis is to obtain useful information about the Circuit-Under-Test (CUT) based on limited excitations and measurements on CUT. The resulting information benefits not only testing engineers and instrumentation operators, but also design engineers and field engineers who could correct their design or manufacturing process, thus reducing Time-To-Market (TTM) and Time-To-Volume (TTV), increasing production yield, and reducing system cost. Generally speaking, analog and mixed-signal test and fault diagnosis consist of three tasks. The first task is **fault detection** which is to check if the CUT is faulty by comparing its responses with responses of a fault-free circuit (gold circuit) under the same excitations. This task is a go/not-go operation, which is usually called **test** in industry. In this task, excitations and measurements as few as possible are required to cover as many as possible faults. If the CUT is judged faulty, the second task is **fault location** to find out where the faulty parameters are within this faulty circuit. This task is dominant for analog and mixed-signal test and fault diagnosis, and distinct methodologies were developed to address this problem. Based on the results of fault location, the final task is **parameter evaluation** to compute how much the faulty parameters are deviated from their nominal values, and how much deviation can be observed among other circuit parameters such as nodal voltages and branch currents.

1.1. History

Analog and mixed-signal test and fault diagnosis always accompany design, manufacture, and maintenance of analog circuits. In the era of discrete analog components, the task of test and fault diagnosis is simple and easy, mostly depending upon the testing engineers' detailed knowledge about analog circuit's operational characteristics and their experiences in analog test and fault diagnosis. In the 1960s, research on this topic was rare, not a systematic exploration. With volume production and widespread application of commercial analog integration circuits (IC), research on analog and mixed-signal test and fault diagnosis became an important area in the 1970s. Numerous methodologies have been designed to meet distinct requirements for analog circuits' specification, model, function, and structure. Several good periodical reviews on this topic appeared in 1979 [1], 1985 [2], 1991 [3] and 1998 [4], respectively.

Recently, with astounding achievements of semiconductor integration and computer-aided software technologies, there is an urgent need for effective, highly automated, systematic solutions to analog and mixed-signal test and fault diagnosis. It is not surprising to observe that there is a steady growth in the number of journal articles and conference/workshop papers addressing problems in analog test and fault diagnosis. More and more professional workshops and special journal issues are also devoted to this area. The papers [5-30] are examples of research efforts since 1997. Review of these papers is in later chapter of this dissertation.

1.2. Significance

After researchers and engineers have paid more attention to digital test during the past three decades, their focus recently switches more to analog and mixed-signal test and fault diagnosis. The driving forces behind this change of focus came from economic considerations and modern technology advances. Economic consideration is the most important factor influencing the motivations for analog and mixed-signal test and fault diagnosis. Like digital test, test cost is a large fraction of the whole cost for design, manufacture and maintenance. Without effective, systematic techniques for analog test and diagnosis, analog test cost could be a dominant fraction of test cost for the whole system. This is even true when analog parts only occupy a small portion of mixed-signal system. Eventually, disproportionate product failure and yield losses will result. Simultaneously, more and more strict requirements to reduce time-to-market and time-to-volume also urge the development of fast and efficient test algorithms to reduce test time. Driven by these economic considerations, mostly from industry, research efforts to look for effective methodologies of analog and mixed-signal test and fault diagnosis are being actively developed now.

Another motivation is coming from modern technology advances. First, it is the development of semiconductor technology that results in such products with high integration density as analog VLSI chips, large scale mixed-signal systems, and System-on-Chip (SoC) solutions. Due to the unbeatable advantages of high speed, analog VLSI chip is the most promising candidate for any area in which the speed is the dominant design specification such as front-end RF circuits in communication, wireless

networking, internet, GPS navigation, real-time control systems, multimedia, artificial intelligence (AI) and information technology (IT). A newly developed technology, system-on-chip, is obtaining popularity in academia and industry. It integrates the whole system (processor, memory and peripherals) into one chip which includes electronic parts (analog and digital hybrid parts), mechanical parts, and even embedded software. As a consequence, the design, manufacture, and maintenance of such systems require corresponding techniques for testing and fault diagnosis. New challenges such as increased complexity, increased die size and reduced accessibility are posed on the problems of analog and mixed-signal test and fault diagnosis.

Secondly, development of computer-aided design tools allowed designers to design more and more complicated circuits. However, corresponding test and diagnosis techniques for analog parts did not improve at the same level. The commercial software devoted to analog circuits still stays on the simulation level such as PSpice, Saber, Smash, etc. The available commercial design and simulation software could satisfy test and diagnosis requirement to some extend by systematic checks and verification of the design process. But insufficient development of test and diagnosis tools (relative to automated design tools) obviously hampers further development of advanced electronic products. Without specialized effective testing and fault diagnosis techniques for analog circuits, the system implementation, time-to-market, and time-to-volume of such products are in significant jeopardy.

Thirdly, digital test can be concluded as successful and mature comparing with analog test and fault diagnosis. Fault models such as stuck-at-1 and stuck-at-0 models which represent the most fault mechanisms encountered in digital circuits have been

widely accepted for a long period. Test strategies, test buses or standards such as Design-for-Testability (DFT) and Built-In-Self-Test (BIST) were proven effective in terms of circuit area, test time, and test cost. Particularly, the IEEE 1149.1 standard for digital boundary-scan test gains more and more supports from industry, so that most of digital products could be effectively tested based on this standard. Computer-aided digital testing software is available commercially and digital Automated Test Equipment (ATE) is widely utilized in manufacturing process of digital products. It is the significant success of digital test that transfers the problem of mixed-signal test to be dominated by the problems of analog test and diagnosis, while digital portions within a mixed-signal system can be easily tested by their domain specific technologies. Based on such assumption, the research focus in this dissertation is on analog test and fault diagnosis.

All of these advances in the techniques for semiconductor integration, automated design, and digital test, together with economic considerations reluctantly witness the falling behind of the analog and mixed-signal test and fault diagnosis. The significant improvement in the automation level of analog and mixed-signal design, test, and fault diagnosis are expected to bridge the gaps with the techniques for digital design, integration and test. In 1998, IEEE proposed the 1149.4 standard for mixed-signal test bus, in order to standardize the process of analog and mixed-signal test and fault diagnosis. But it is only one of attempts to address the problem of analog and mixed-signal test and fault diagnosis, and has not yet gained enough support from industry. Different voices can also be heard from academia about this standard. It does not enjoy the similar success level like its counterpart – IEEE 1149.1 standard for boundary scan in digital test area. There is still a long way for the emergence of a widely accepted standard

or strategy in analog test and fault diagnosis. In general, there is an urgent and growing need to develop methodologies and software tools for analog test and fault diagnosis.

1.3. Objectives of the Dissertation

Based on the assumption that mixed-signal system is decomposed into separated analog, digital and software blocks, the scope of this dissertation is in the area of analog test and fault diagnosis.

Facing up the fact that there is no general paradigm in analog test and diagnosis, the primary objective of the dissertation research is exploring a computer-aided test and diagnosis methodology or strategy applicable to general analog systems. The challenging test problems happened in most of analog systems including ambiguities, complexity, accessibility, catastrophic faults and model building are on the top list of the dissertation research. The computer-aided solution to analog test and fault diagnosis is to improve the efficacy and automation level of the test methodologies. Thus, the research results could be programmed and embedded into simulator or ATE test program.

The subject is a continuous-time, time-invariant, analog system under stable state. Independent measurements are limited, so that an obvious identification of faults cannot be guaranteed. The primary task in dissertation research is to address ambiguities problem in analog fault diagnosis. Firstly, the analog system can be described in matrix format by circuit analysis and measurement. Hence this system description matrix is determined by parameter values, parameter locations (or circuit topology) and measurements. When faults occur, the value changes of faulty parameters and their

corresponding locations must be reflected in system description matrix in terms of dependency/independency, and/or consistency/inconsistency relations among matrix elements. Then, the dissertation research is to find out an approach to efficiently extract the ambiguities hidden in system description matrix to identify the faults and implement the aims of analog test and diagnosis.

The other tasks in dissertation work include exploring complexity and accessibility problems through decomposing large system into smaller subsystems, and considering special test cases – catastrophic faults location. The significance of this dissertation work is to provide a efficient and systematic paradigm for general-background analog test and fault diagnosis.

1.4. Classification

The existing techniques for analog and mixed-signal test and fault diagnosis come from different research efforts with distinct goals to satisfy the requirements for specification, function, or model. The most straightforward technique is to ensure that the circuit meets all the specification requirements provide by the design engineers. This is called specification-based test technique. The test inputs are generated directly from the specifications. Thus, a circuit passing test process will surely meet the specifications. However, this technique is extremely expensive because the number of specifications is usually huge even for small analog circuits.

Another technique is to verify that the circuit meets the desired functional requirements. This is called functional-based test technique [4, 50]. It is very effective for

digital test since digital circuits satisfying desired function will meet the performance requirements. But most of specifications of analog circuits are not function-based. It is possible for an analog circuit to function correctly without meeting performance specifications. This is one of the peculiarities of analog circuits which result from its highly nonlinear behavior.

One idea is to build models for specific faults encountered in the process of design, manufacture and operation. This is called model-based technique [3-4, 50]. Since until now no effective fault model can cover most of fault mechanisms, no direct relation between fault coverage and specification satisfaction can be established. Therefore, this technique is only effective for specific faults, not for the faults not covered by the fault model.

Analog and mixed-signal test and fault diagnosis can also be divided into two categories according to the number of faults: single fault and multiple-fault [2-4]. Single fault is the most common case occurred in practice. Multiple-fault case usually happens as a consequence of a serious single fault. For example, a short-circuit fault may result in a strong current and cause the failure of other circuit components. Multiple-fault is more difficult to model and detect, particularly in the presence of tolerance or a measurement noise. In addition, in a multiple-fault situation, one fault's effect on the circuit could be masked by the effects of other faults. The research in this dissertation addresses a multiple-faults diagnosis.

In this dissertation, a popular classification proposed by Bandler [2] is used, which categorizes the analog and mixed-signal test and fault diagnosis according to the stage in testing process at which simulation of the tested circuit occurs: Simulation-

Before-Test (SBT) and Simulation-After-Test (SAT) approach. Fig. 1.1 illustrates the different techniques according to this classification in [2].

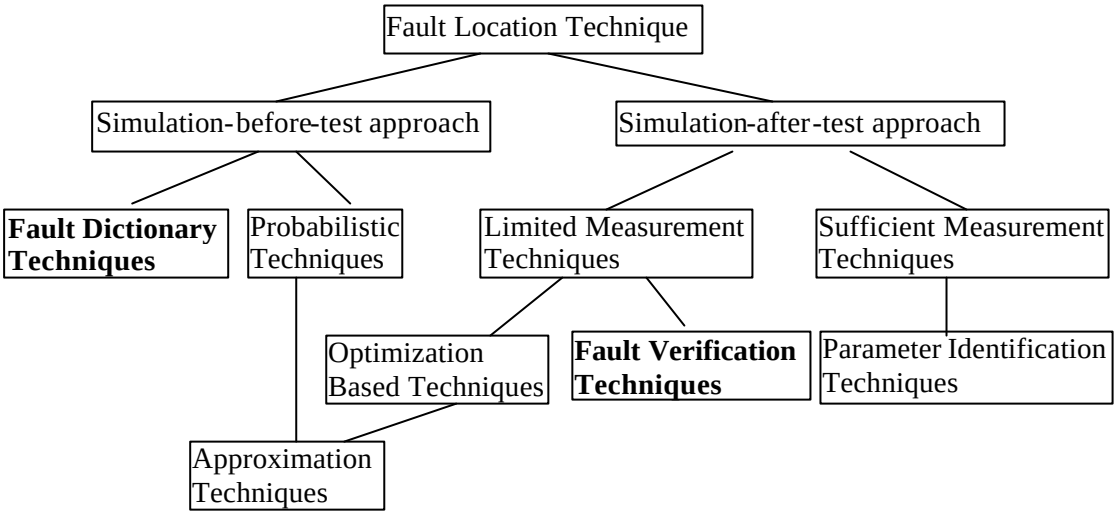

Figure 1.1 Classification of analog test and fault diagnosis [2]

Fault dictionary technique is the most popular methodology under the Simulation-Before-Test approach. It has wide applications in digital test, in which the responses of circuit under test are compared with a set of pre-stored outputs on the ATE. Similarly, analog circuits are analyzed and most likely faults are collected into the look-up table, or a dictionary. Then the circuit for each case of specific faults is simulated with chosen stimuli, and the corresponding responses are also stored in the dictionary. To achieve the required degree of diagnosability, optimum measurements are selected. In the process of testing, responses of the CUT are compared with signatures stored in the dictionary. Fault location is implemented by criteria based on pattern recognition methods. There are three

dominant methods in constructing a fault dictionary for analog circuits: DC, frequency domain, and time domain approaches. Efficient fault simulation and optimum selection of measurements play very important role in the dictionary method.

Approximation technique is based on the optimization theory. Although a limited number of measurements is needed, on-line simulation (and thus extensive on-line computation) is required for fault location. The most likely fault parameters are located according to certain fault locating criteria. Due to the nature of this technique, the exact solution to fault location and parameter evaluation cannot be obtained. Therefore the application of such kind method is limited.

Fault verification technique is a practical and promising solution to the problems of analog test and fault diagnosis. When the number of faults is limited and the number of independent measurements is greater than the number of faults, verification techniques are effective based on known information such as circuit topology, nominal circuit parameters and nodal voltage measurements.

The most attractive feature of parameter identification technique is that it can provide solution to the values of all circuit parameters within faulty circuit. The faulty parameters are consequently located by checking which circuit parameters are beyond the design tolerance margins. Circuit topology and nominal values of all circuit parameters are assumed known. Only a part of the circuit nodes is accessible for measurement. The necessary condition for parameter identification technique is that enough independent measurements must be used. This leads to an unavoidable disadvantage for this technique: too many accessible nodes are required for independent measurements, which is not practical for analog circuits with high integration density and limited accessibility.

Considering both advantages and disadvantage of above four techniques, fault dictionary and fault verification techniques are the most promising solutions to practical problems in analog test and fault diagnosis. Most of research efforts from industry and academia are located within dictionary and verification categories. In this dissertation, techniques of fault dictionary, fault verification including decomposition methods are involved to address the problems in analog test and diagnosis.

1.5. Problems in Analog Test and Fault Diagnosis

Fig. 1.2 is a typical diagram of analog and mixed-signal system. Most of tasks are processed by digital units. This is a trend in today's market of mixed-signal products. Although analog units are relatively less numerous than digital in modern electronics, they cannot be completely replaced by digital units completely because the real world is talking in analog signals. Analog units such as filter, sample-and-hold (S&H), analog-to-

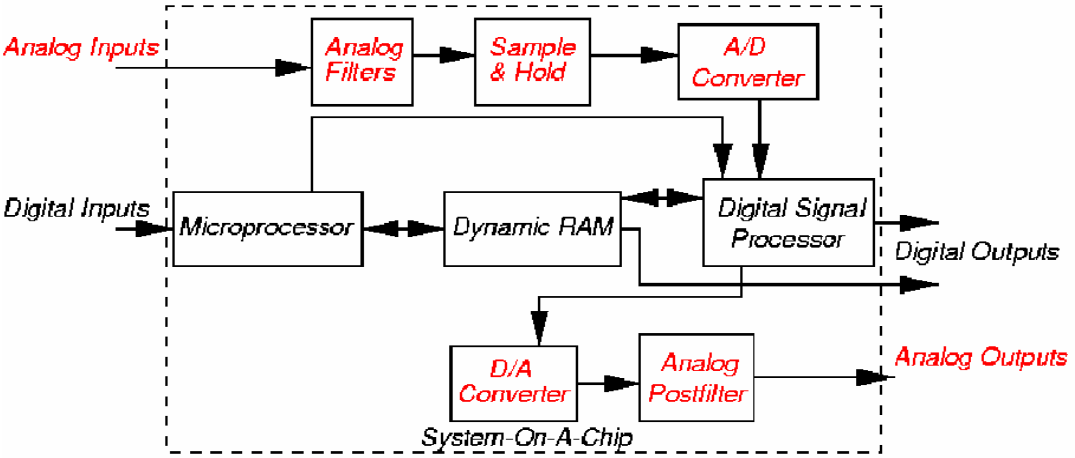

Figure 1.2 Diagram of analog and mixed-signal system

digital converter (ADC), digital-to-analog converter (DAC), and phase-locked-loop (PLL) are utilized as interfaces between digital processing units and the real world. High frequency communication signals, radio transmitters, TV broadcast, etc, are using modulated analog signals for transmission, perhaps transmitting digital information.

In order to test an individual analog unit within such a mixed-signal system, all available information about circuit-under-test is collected. Circuit topology and nominal circuit parameters can be obtained from manuals or design engineers. Excitations and responses can be measured. Based on these known information, the task of test and fault diagnosis is to obtain useful information about faults by different circuit analysis and information extraction techniques (Fig. 1.3).

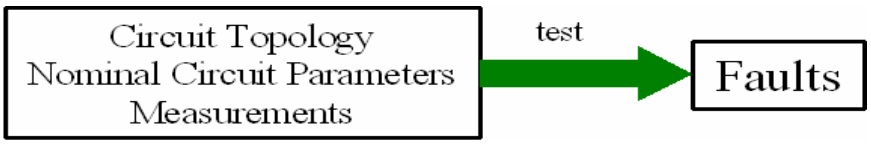

Figure 1.3 Diagram of analog and mixed-signal test and fault diagnosis

The difficulties of analog test and fault diagnosis lie in inherited features of analog circuits. The first challenging problem is ambiguities which prevent accurate measurement and accurate computation. Examples of ambiguities include circuit parameter tolerance, limited measurements and non-linearity of analog circuits. Even for a linear circuit, the deviation of circuit parameters from their nominal values will lead to the nonlinear relationship between the circuit responses and changes in the component

values. With the popularity of SoC, circuit complexity is significantly increased while accessibility is relatively reduced. Universally accepted, effective analog fault model to establish a relation between fault coverage and circuit performance is still lacking. Fast and efficient computation algorithms are also greatly needed for analog simulation and building up analog models.

Due to above difficulties in analog test and fault diagnosis, analog test cost is significantly increasing. Table 1.1 is the average cost for one ATE according to statistical data in 2000: $ 4.272 M to buy one ATE and $ 1.439 M to operate this ATE [31].

Table 1.1 Cost of manufacturing testing in 2000AD [31]

▪ 0.5-1.0GHz, analog instruments,1,024 digital pins: ATE purchase price = $1.2M + 1,024 x $3,000 = **$4.272M**
▪ Running cost (five-year linear depreciation) = Depreciation + Maintenance + Operation = $0.854M + $0.085M + $0.5M = **$1.439M/year**
▪ Test cost (24 hour ATE operation) = $1.439M/(365 x 24 x 3,600) = **4.5 cents/second**

Table 1.2 shows the developing trends of IC fabrication [32]. ATE is becoming more and more expensive because semiconductor products will become more and more complicated in terms of circuit complexity, pin number, clock rate, power consumption, etc.

Table 1.2 Current and future development of IC fabrication [32]

	1997 -2001	**2003 - 2006**	**2009-2012**
Feature size (micron)	0.25 - 0.15	0.13 - 0.10	0.07-0.05
Transistors/sq. cm	4 - 10M	18 - 39M	84-180M
Pin count	100 - 900	160 - 1475	260-2690
Clock rate (MHz)	200 - 730	530 - 1100	840-1830
Power (Watts)	1.2 - 61	2 - 96	2.8-109

In this dissertation, all above problems are touched on and at least one solution facing general background analog systems is provided for each problem. Fault verification based on ambiguity group locating technique is described in Chapter 2 to address the problem of ambiguities resulting from limited measurement for the purpose of accurate computation. To reduce complexity, Chapter 3 illustrates how to decompose a large scale system into smaller sub-systems in order to reduce system complexity. Simultaneously, nodal voltages on some specific inaccessible nodes can be calculated. Thus, accessibility to its systems is relatively increased. Based on a stuck fault model, a multiple-stuck-fault location technique is implemented in Chapter 4 to eliminate the requirement for repetitive simulations in traditional stuck-fault location techniques. Conclusions are given in Chapter 5.

CHAPTER 2 FAULT VERIFICATION FOR ACCURATE COMPUTATION

2.1. Ambiguity and Verification

One of the reasons for ambiguities in analog test and fault diagnosis is a limited number of independent measurements. Fault verification technique is effective for accurate computation to address the problem of limited measurements. As stated in Section 1.4, fault dictionary and fault verification techniques are the most utilized approaches in analog fault diagnosis. Dictionary techniques require huge simulation works [5-7] before test because a complete fault dictionary containing all feasible fault examples cannot obviously be generated due to the continuous nature of the analog parametric faults. That is why dictionary technique usually test and diagnose the single-fault case and catastrophic faults, but not effective for multiple-fault case or parametric faults. Neural network through learning and training processes can supplement this incompleteness problem by sampling the fault space or recognizing the fault patterns [8-10]. As a consequence, the accuracy of fault location and parameter evaluation is limited by those optimization approaches.

Fault verification is a promising solution to solve limited measurements and computation accuracy problems in analog test and fault diagnosis. The basic requirement is that a few parameters are faulty while the remaining parameters are within design tolerance specifications. Specifically speaking, the number of measurements required is less than the number of circuit nodes or circuit parameters, but greater than the number of

faults in a faulty circuit. The circuit topology is assumed known, thus the graph theory can be utilized to locate faulty parameters. The nominal values of circuit parameters are also supposed known to facilitate the application of network theory and mathematical methods in the fault location. Only the voltage measurements are needed, which reduces the error introduced by measurement instrumentation. All of these requirements are easily satisfied in practice. The idea behind fault verification technique is to check the consistency of certain equations which are invariant to the changes in faulty parameters. Since this technique checks whether a certain subset of circuit parameters can be faulty or not based on the assumption that the circuit is faulty, it is referred to as a verification technique.

In [11-12], a verification technique was developed for single-fault diagnosis in piecewise linear analog circuits based on homotopy approach and on bilinear transformation. Another verification approach was proposed in [13] for parametric fault diagnosis in linear and non-linear circuits, but its performance is weak when the values of deviations are large. Large change sensitivity analysis was utilized by some researchers [14, 33] in analog fault diagnosis when there are large deviation values of parametric faults. To address the problems of computation round-off and large amount of computations, symbolic analysis was utilized [15-17]. To efficiently recognize the ambiguity groups hidden within the fault diagnosis equation, different ambiguity group locating techniques were proposed for fault verification [18-20, 34]: symbolic analysis was utilized in [18], numerical analysis in [19, 34] and decomposition analysis in [20].

In [21], a fault verification method was proposed for single fault diagnosis in linear analog circuits. Multiple excitations are required and Woodbury formula in matrix

theory is applied to locate the faulty parameter. This method was also applied to multiple fault diagnosis by decomposition technique assuming that each sub-circuit contains at most a single faulty parameter. In this chapter, the fault verification method developed in [21] is generalized and extended to multiple fault diagnosis of linear analog circuits in frequency domain. Ambiguity group determination based on numerical analysis in [19] is modified and used for fault location. Large parametric deviations and open/short faults are considered.

In Section 2.2, Kirchhoff current law (KCL) is applied to each circuit node, together with the constitutive equations for all circuit parameters without admittance description, to obtain the modified nodal equation. Circuit topology is comprehensively described by two structural matrices, and the Woodbury formula is used to construct the fault diagnosis equation. In Section 2.3, a newly developed technique for minimum size ambiguity group locating technique based on QR factorization is applied to detect and identify the multiple faults directly. Only one node is needed for voltage measurement, but multiple excitations and corresponding measurements on this node are required for fault identification. Parameter evaluation is to calculate the exact solution to the deviated values of faulty parameters. Section 2.4 provides example circuits to demonstrate the developed technique. The results are compared with those obtained by the method in [21]. The demonstrated methodology is generalized in Section 2.5 and applied to develop two new techniques for multiple fault diagnosis. Simultaneously, an advanced research on this verification technique is explored in order to remove Gaussian elimination and swapping operations based on multiple excitations and multiple measurements. Example

circuit is used to verify this approach. In Section 2.6, the developed techniques are summarized.

2.2. Woodbury Fault Verification Technique

Generally, circuit topology as well as its parameters' nominal values are known. Consider a continuous-time, time-invariant, strongly connected, linear circuit with $n+1$ nodes and p parameters. The $(n+1)^{th}$ node , denoted by zero, is assigned to be the grounded reference node while the remaining n nodes are ungrounded. All p parameters are divided into two categories: one contains parameters which have admittance description such as conductance, capacitor and voltage-controlled-current source, another contains parameters which have no admittance description such as impedance, inductor, current-controlled-source, operational amplifier, etc.

Applying the KCL to each circuit node, one can obtain n equations with variables being nodal voltages and parameter currents. Constitutive equations in terms of nodal voltages and parameter currents, which define the characteristics of all parameters without admittance description, are appended to the above n KCL-based equations, thus the system's equations are constructed in the following form:

$$T_g X_g = W_g \tag{2.1}$$

where T_g is a gxg coefficient matrix consisting of circuit parameters, X_g is a $gx1$ solution vector of node voltage and parameter currents, and W_g is a $gx1$ excitation vector composed of independent current and voltage sources, and initial conditions of

capacitors and inductors. The first n rows in T_g, X_g and W_g correspond to n nodes. The resulting system equation (2.1) is called the ***modified nodal equation*** in [35]. Note that $g=n$ for normal nodal analysis of a circuit in which all parameters have admittance description, and $g>n$ for modified nodal analysis of a circuit in which some parameters have non-admittance description. Provided that the circuit functions in a stable state, the parametric values of nodal voltages and parameter currents are finite and unique. The coefficient matrix T_g is non-singular since the circuit is a strongly connected network.

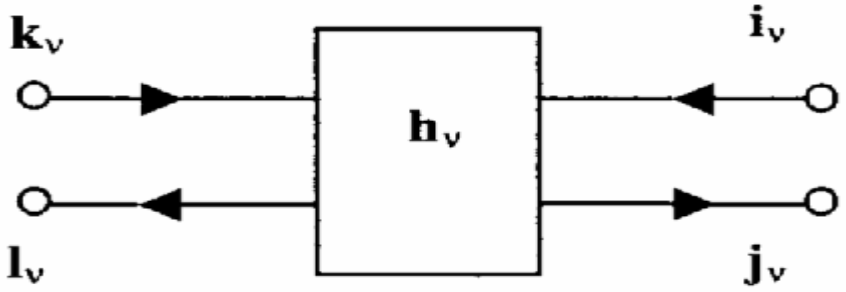

Figure 2.1 Model of parameter location

One important fact about circuit topology is that each circuit parameter, say h_ν $(\nu = 1, 2, \ldots, p)$, can be located by at most 4 circuit nodes as indicated in Fig. 2.1: 2 input nodes k_ν and l_ν, and 2 output nodes i_ν and j_ν. The current orientations are also indicated in Fig. 2.1. For 2-terminal parameters such as resistor and capacitor, the input nodes will be the same as the output nodes: $k_\nu = i_n$ and $l_\nu = j_n$. Based on this fact, the

circuit topology can be completely described by two *gxp* structural matrices *P* and *Q* which are defined as follows:

$$P=\left[p_1\ p_2\ \ldots p_p\right]=[e_{i_1}-e_{j_1}\ \ e_{i_2}-e_{j_2}\ \ \ldots\ \ e_{i_p}-e_{j_p}\ ]$$
$$Q=\left[q_1\ q_2\ \ldots q_p\right]=[e_{k_1}-e_{l_1}\ \ e_{k_2}-e_{l_2}\ \ \ldots\ \ e_{k_p}-e_{l_p}\ ] \qquad (2.2)$$

where e_n represents a *gx1* vector of zeros except for the v^{th} entry, which is equal to one, and p_n and q_n represent *gx1* vectors describing the locations of output nodes and input nodes, respectively. Matrices *P* and *Q* are only determined by the locations, not the values of the circuit parameters. The columns of matrix *P* correspond to the locations of the output nodes of circuit parameters while the columns of matrix *Q* correspond to the locations of the input nodes of circuit parameters.

Another important fact is that most parameters in linear circuits will enter the coefficient matrix T_g in the symbolic form

$$\begin{array}{c} \\ i_n \\ j_n \end{array}\begin{array}{c} \begin{array}{cc} k_n & l_n \end{array} \\ \begin{bmatrix} h_n & -h_n \\ -h_n & h_n \end{bmatrix} \end{array} \qquad (2.3)$$

with the equivalent algebraic representation being

$$\left(e_{i_n}-e_{j_n}\right)h_n\left(e_{k_n}-e_{l_n}\right)^T=p_n\,h_n\,q_n^T \qquad (2.4)$$

where superscript *T* denotes transpose of a matrix or a vector. For any grounded node, the corresponding row or column in the symbolic form will be removed together with the corresponding unit vector e_n in the algebraic form. Resistor, inductor, capacitor,

dependent sources, and operational amplifier with its negative inverse gain being a parameter are examples of circuit devices described in this way. In this chapter, all faulty parameters are restricted to such type of circuit devices.

Apply (2.1) to fault-free and faulty circuit, respectively, with the same excitation sources to get

$$T_0 X_0 = W_0 \tag{2.5}$$

$$TX = (T_0 + \Delta T)(X_0 + \Delta X) = W_0 \tag{2.6}$$

where

$$T = T_0 + \Delta T \tag{2.7}$$

$$X = X_0 + \Delta X \tag{2.8}$$

Suppose that the first f of p parameters are faulty and are changed from their nominal values $h_{10}, h_{20}, ..., h_{f0}$ to the new values $h_1 = h_{10} + d_1$, $h_2 = h_{20} + d_2$, ..., $h_f = h_{f0} + d_f$, where $d_1, d_2, \ldots, d_f$ are the parameter deviations and the deviation vector d is an *fx1* vector:

$$d = [d_1 \; d_2 \; \ldots \; d_f]^T \tag{2.9}$$

Define F as the faulty parameter set, and assume that each faulty parameter F_v $(v = 1, 2, \ldots, f)$ is located on intersection of the corresponding rows i_v and j_v and columns k_v and l_v of the coefficient matrix T. The deviation of the coefficient matrices now has the following form:

$$\Delta T = \sum_{n=1}^{f} p_v d_n q_n^T = P_f \; diag \; (d) \; Q_f^T \tag{2.10}$$

where $diag(d)$ is an *fxf* diagonal matrix and P_f and Q_f are *gxf* matrices which contain 0 and ± 1 entries:

$$\begin{aligned} P_f &= [p_1 \; p_2 \; \ldots p_f] = [e_{i_1} - e_{j_1} \quad e_{i_2} - e_{j_2} \quad \ldots \quad e_{i_f} - e_{j_f}] \\ Q_f &= [q_1 \; q_2 \; \ldots q_f] = [e_{k_1} - e_{l_1} \quad e_{k_2} - e_{l_2} \quad \ldots \quad e_{k_f} - e_{l_f}] \end{aligned} \tag{2.11}$$

Note that P_f and Q_f are sub-matrices of P and Q respectively. They can be constructed from P and Q by selecting all columns in P and Q corresponding to faulty parameters.

The solution vector for fault-free circuit is

$$X_0 = [x_{1,0} \; x_{2,0} \; \ldots \; x_{g,0}]^T \tag{2.12}$$

where subscript *0* indicates that the denoted parameters are for fault-free circuit. Hence the product of Q_f^T and X_0 can be written as

$$\begin{aligned} Q_f^T X_0 &= [e_{k_1} - e_{l_1} \quad e_{k_2} - e_{l_2} \quad \ldots e_{k_f} - e_{l_f}]^T X_0 \\ &= [x_{k_1,0} - x_{l_1,0} \; x_{k_2,0} - x_{l_2,0} \; \ldots \; x_{k_f,0} - x_{l_f,0}]^T \\ &= [x_{k_1 l_1,0} \quad x_{k_2 l_2,0} \; \ldots \; x_{k_f l_f,0}]^T \end{aligned} \tag{2.13}$$

and it has the physical interpretation of controlling nominal signal values (e.g. voltages) on faulty parameter input terminals. Applying the Woodbury formula [36] in matrix theory

$$\left(A + PS^{-1}V\right)^{-1} = A^{-1} - A^{-1}P\left(S + VA^{-1}P\right)^{-1}VA^{-1} \tag{2.14}$$

to (2.7) and (2.10) with $A=T_0$, $S^{-1} = diag\ (d\ )$, $P=P_f$ and $V = Q_f{}^T$, the inverse of coefficient matrix T has the following form:

$$\begin{aligned} T^{-1} &= \left(T_0 + P_f\ diag(d)\, Q_f{}^T\right)^{-1} \\ &= T_0{}^{-1} - T_0{}^{-1} P_f \left(diag(d^{-1}) + Q_f{}^T T_0{}^{-1} P_f\right)^{-1} Q_f{}^T T_0{}^{-1} \end{aligned} \tag{2.15a}$$

The value of d_n $(n = 1, 2, \ldots, f)$ cannot be zero or infinity to meet the requirements of inverting restrictions in the Woodbury formula. Since d_n being zero means fault-free parameter, and only faulty parameters will be identified by following fault diagnosis algorithm, only one restriction is resulted: d_n cannot be infinite, which corresponds to the case of open admittance or short impedance. But open or short faults can be dealt with by ideal switch introduced in modified nodal analysis [35]. Therefore, the proposed method can handle open and short faults as well.

Let us define

$$\begin{aligned} b &= [\,b_1 \quad b_2 \quad \ldots \quad b_n\,]^T = T_0{}^{-1} P_f \\ g &= Q_f{}^T T_0{}^{-1} P_f \end{aligned} \tag{2.16}$$

then (2.15a) has following form

$$T^{-1} = T_0{}^{-1} - b\left(diag(d^{-1}) + g\right)^{-1} Q_f{}^T T_0{}^{-1} \tag{2.15b}$$

Since the coefficient matrices T_0 and T are non-singular, the solution vector for faulty circuit X is then obtained using (2.6) and considering (2.15b) and (2.5):

$$\begin{aligned} X &= T^{-1} W_0 \\ &= T_0{}^{-1} W_0 - b\left(diag\,(d^{-1}) + g\right)^{-1} Q_f{}^T T_0{}^{-1} W_0 \\ &= X_0 - b\left(diag\left(d^{-1}\right) + g\right)^{-1} Q_f{}^T X_0 \end{aligned} \tag{2.17}$$

Thus, the deviation vector ΔX can be obtained by (2.8) considering (2.17) and (2.13):

$$\begin{aligned}\Delta X &= X - X_0 \\ &= -b\left(diag\left(d^{-1}\right)+g\right)^{-1} Q_f^T X_0 \\ &= \begin{bmatrix} a_{11} & a_{12} & \dots a_{1f} \\ a_{21} & a_{22} & \dots a_{2f} \\ \dots\dots & & \\ a_{g1} & a_{g2} & \dots a_{gf} \end{bmatrix} \begin{bmatrix} x_{k_1 l_1,0} \\ x_{k_2 l_2,0} \\ \dots \\ x_{k_f l_f,0} \end{bmatrix}\end{aligned} \tag{2.18}$$

where

$$\begin{aligned}a &= -b\left(diag\left(d^{-1}\right)+g\right)^{-1} \\ &= \begin{bmatrix} a_{11} & a_{12} & \dots a_{1f} \\ a_{21} & a_{22} & \dots a_{2f} \\ \dots\dots & & \\ a_{g1} & a_{g2} & \dots a_{gf} \end{bmatrix} = \begin{bmatrix} a_1 \\ a_2 \\ \dots \\ a_g \end{bmatrix}\end{aligned} \tag{2.19}$$

Usually, voltage measurements are easier to carry out and are less invasive to analog circuit properties than current measurements. Therefore, only nodal voltage measurements are used in this technique. Suppose the i^{th} node is accessible for measurement, then by (2.18):

$$\Delta X_i = [a_{i1}\ a_{i2}\ \dots a_{if}][x_{k_1 l_1,0}\ x_{k_2 l_2,0}\ \dots\ x_{k_f l_f,0}]^T \tag{2.20}$$

According to definition of *gxf* matrix a in (2.19) and (2.16), matrix a does not dependent on the location of the excitation sources. Thus matrix a is invariant when applying the multiple excitation method, i.e., the same coefficients a_{ij} link deviation of

measurements ΔX_i and nominal signal values at the location of faulty parameter $x_{k_j l_j}$ independently on the excitation vector applied. After measuring the corresponding nodal voltages at the i^{th} node with m independent excitation vectors $W_e\,(e = 1,2,...,m)$, following equations are then obtained

$$\begin{aligned}
\Delta X_i^{(1)} &= [a_{i1}\ a_{i2}\ ...a_{if}\ ][x^{(1)}_{k_1 l_1,\,0}\ x^{(1)}_{k_2 l_2,\,0}\ \dots\ x^{(1)}_{k_f l_f,\,0}]^T \\
\Delta X_i^{(2)} &= [a_{i1}\ a_{i2}\ ...a_{if}\ ][x^{(2)}_{k_1 l_1,\,0}\ x^{(2)}_{k_2 l_2,\,0}\ \dots\ x^{(2)}_{k_f l_f,\,0}]^T \\
&\cdots\cdots \\
\Delta X_i^{(m)} &= [a_{i1}\ a_{i2}\ ...a_{if}\ ][x^{(m)}_{k_1 l_1,\,0}\ x^{(m)}_{k_2 l_2,\,0}\ \dots\ x^{(m)}_{k_f l_f,\,0}]^T
\end{aligned} \tag{2.21}$$

or in a matrix form

$$\begin{aligned}
\Delta X_i^{M} &= \begin{bmatrix} \Delta X_i^{(1)} \\ \Delta X_i^{(2)} \\ \cdots\cdots \\ \Delta X_i^{(m)} \end{bmatrix} = \begin{bmatrix} x^{(1)}_{k_1 l_1,\,0} & x^{(1)}_{k_2 l_2,\,0} & \dots & x^{(1)}_{k_f l_f,\,0} \\ x^{(2)}_{k_1 l_1,\,0} & x^{(2)}_{k_2 l_2,\,0} & \dots & x^{(2)}_{k_f l_f,\,0} \\ \cdots\cdots & & & \\ x^{(m)}_{k_1 l_1,\,0} & x^{(m)}_{k_2 l_2,\,0} & \dots & x^{(m)}_{k_f l_f,\,0} \end{bmatrix} \begin{bmatrix} a_{i1} \\ a_{i2} \\ \cdots \\ a_{if} \end{bmatrix} \\
&= X_b^{MF} a_i
\end{aligned} \tag{2.22}$$

where superscript *M* denotes the set of multiple excitations and m is the number of these excitations. Since each single measurement node can be one of the nodes used for multiple excitation method, then the total number of accessible nodes should be *m*. Assume that $f \le m-1 \le p$, then the coefficient matrix X_b^{MF} has more rows than columns which is necessary to guarantee the uniqueness of solution to (2.22) with test verification. This ability to verify results of fault diagnosis is unique for the fault verification techniques (hence their names). In addition, fault verification techniques give

exact solutions even with large (catastrophic) faults, which is also unique in analog fault diagnosis. Equation (2.22) establishes a linear relationship between the measured responses of the faulty circuit ΔX_i^M and the faulty parameter deviations d (since according to (2.19), vector a_i is a linear function of d) Therefore (2.22) is called **Woodbury fault diagnosis equation**, and the coefficient matrix X_b^{MF} is called **Woodbury fault diagnosis matrix**.

2.3. Fault Diagnosis in Woodbury Fault Verification Technique

Testability is not the focus of this dissertation. Therefore an assumption is made that the given measurement set can give at least one finite solution to circuit parameters.

2.3.1. Fault Detection

As the first stage of fault diagnosis, fault detection is easily implemented. If the measurement deviation vector ΔX_i^M in the fault diagnosis equation is a zero vector, then the CUT is judged as fault-free for the given excitation and measurement sets. Otherwise, at least one fault is judged detected by the given measurement set.

2.3.2. Fault Identification

To identify the faulty parameters, first let us analyze the fault diagnosis equation. The left-side of (2.22) is a known vector from measurements, the right side is the product

of an unknown coefficient matrix X_b^{MF} and an unknown solution vector a_i. According to (2.13), matrix X_b^{MF} is determined by faulty parameter locations and X_0, is a solution vector for fault-free circuit. Hence the columns in X_b^{MF} represent the differences between the nominal values of nodal voltages or parameter currents across the 2 input nodes of the faulty parameters. Although matrix X_b^{MF} is unknown, but all of the nodal voltages and parameter currents in fault-free circuit are really known! Similar as in (2.13), a new *mxp* matrix X_b^{MP} is constructed as follows

$$\begin{aligned} Q^T X_0 &= [e_{k_1} - e_{l_1} \;\; e_{k_2} - e_{l_2} \;\; \ldots e_{k_p} - e_{l_p}]^T X_0 \\ &= [x_{k_1,0} - x_{l_1,0} \;\; x_{k_2,0} - x_{l_2,0} \;\; \ldots x_{k_p,0} - x_{l_p,0}]^T \\ &= [x_{k_1 l_1,0} \;\; x_{k_2 l_2,0} \;\; \ldots \;\; x_{k_p l_p,0}]^T \end{aligned} \tag{2.23}$$

$$X_b^{MP} = \begin{bmatrix} x_{k_1 l_1,0}^{(1)} & x_{k_2 l_2,0}^{(1)} & \cdots & x_{k_p l_p,0}^{(1)} \\ x_{k_1 l_1,0}^{(2)} & x_{k_2 l_2,0}^{(2)} & \cdots & x_{k_p l_p,0}^{(2)} \\ \ldots\ldots & & & \\ x_{k_1 l_1,0}^{(m)} & x_{k_2 l_2,0}^{(m)} & \cdots & x_{k_p l_p,0}^{(m)} \end{bmatrix} \tag{2.24}$$

where superscript *P* denotes the set of all circuit parameters. Each column of X_b^{MP} corresponds to one circuit parameter. Apparently, fault diagnosis matrix X_b^{MF} is a sub-matrix of X_b^{MP}, which can be constructed by collecting all columns in X_b^{MP}

corresponding to the faulty parameters. Matrix X_b^{MF} has more rows than columns whereas X_b^{MP} has less rows than columns due to the restriction $f \le m-1 \le p$.

For the purpose of fault identification, it is necessary to find out which set or sets of columns in X_b^{MP} can satisfy the fault diagnosis equation, i.e., find the dependency between ΔX_i^M and the desired set(s) of columns in X_b^{MP}. It is very possible that there are more than one qualifying sets, so it is regulated in this chapter that the minimum size of the column set satisfying fault diagnosis equation will be the desired coefficient matrix in fault diagnosis equation. One obvious way is to have a combinatorial search through all columns in X_b^{MP}, which is the traditional way in fault verification technique [2] and requires the number of operations $O\left(\sum_1^f \binom{p}{i}\right)$ for limited faults among p parameters, thus it is computationally costly. More efficient method for fault identification is expected to reduce the computational cost. Our idea is to transform fault identification problem into a mathematical problem: locating the minimum size ambiguity group which satisfy the fault diagnosis equation. Ambiguity group is defined as a set of parameters corresponding to linearly dependent columns of X_b^{MP} which, in general case, does not give a unique solution in fault identification. However, in this work it will be shown how the set of faulty parameters can be identified by finding ambiguity groups.

In [19], a method was developed to locate the minimum size ambiguity groups by using a linear combination matrix C (which will be introduced later) with minimum

number of non-zero entries. In this chapter, the method in [19] is modified to identify dependence of the measurement vector ΔX_i^M on a subset of columns from X_b^{MP}. Gaussian elimination step is introduced, and a minimum size ambiguity group is located by identifying the column with minimum number of non-zero entries in the linear combination matrix *C*. The three steps, Gaussian elimination, QR factorization and swapping performance are detailed next.

2.3.2.1. Gaussian Elimination

First let us denote an augmented *mx(p+1)* matrix B_S as the concatenation of the vector ΔX_i^M and the matrix X_b^{MP}:

$$B_S = [\Delta X_i^M \quad X_b^{MP}] \tag{2.25}$$

Then the first column of matrix B_S will be normalized to have a unit in its first row,

$$\hat{B}_S(i,1) = \frac{B_S(i,1)}{B_S(1,1)}, \quad i = 1,2,\ldots,m. \tag{2.26}$$

If the first entry of matrix B_s, $B_s(1,1)$ happens to be zero, just permute the rows of B_s so that the first entry $B_s(1,1)$ is non-zero. Such a nonzero entry must exist since ΔX_i^M is a non-zero vector for a faulty circuit. Eliminate the remaining entries in the first row of matrix B_S by performing a similar operation to Gaussian elimination as follows:

$$\hat{B}_S(i,\ j) = B_S(i,\ j) - \frac{B_S(i,1)}{B_S(1,1)} B_S(1,\ j), \quad i = 1, 2, ..., m;\ j = 2, 3, ...,\ p+1 \qquad (2.27)$$

Finally, an *mx(p+1)* matrix $\hat{B}_S$ is obtained in the following form:

$$\hat{B}_S = \begin{bmatrix} 1^{1\times 1} & 0^{1\times p} \\ (\Delta\hat{X}_i)^{(m-1)\times 1} & B^{(m-1)\times p} \end{bmatrix} \qquad (2.28)$$

where the superscript represents the size of a vector or a matrix. Matrix B is obtained from X_b^{MP} after elimination the dependence on ΔX_i^{M} and is called a **fault verification matrix**. The dependency among columns of matrix B surely indicate the dependency between ΔX_i^{M} and corresponding columns of matrix X_b^{MP}. Thus the research efforts can only concentrate on the dependencies among the columns of the verification matrix *B*. The fault verification matrix will be used to identify faulty parameters and find their deviations from the nominal values, thus providing us with a fault diagnosis mechanism.

2.3.2.2. QR Factorization

The rank of B determines a maximum number of faults that can be uniquely identified by solving the fault diagnosis equation. Because *m-1<p*, B can be decomposed into two linearly dependent sub-matrices as follows

$$B = [B_1\ B_2] = B_1[I\ C] \qquad (2.29)$$

$$B_2 = B_1 C \qquad (2.30)$$

where *(m-1)xr* matrix B_1 has the full column rank equal to the rank *r* of the matrix *B*, and $r\times(p-r)$ matrix C is called a **linear combination matrix** whose columns expand a set

of basis columns from B_1 into the corresponding columns of B_2. Note that the selection of independent columns of B_1 is not unique, which is an important issue in solving the fault diagnosis equation in the presence of ambiguities. Different partitions define different linear combination matrices *C*.

Since an ambiguity group is a set of circuit parameters corresponding to linearly dependent columns of *B*, a canonical ambiguity group is defined as a minimal set of parameters corresponding to linearly dependent columns of *B*. It means that if any single parameter is removed from the canonical ambiguity group, the remaining set corresponds to independent columns of *B* and is uniquely solvable. A combination of canonical ambiguity groups with at least one common element was defined as ambiguity cluster.

To efficiently deal with the fault verification problem, it is necessary to look for a partition (2.29) with the matrix *C* in a **minimum form**, which is defined as such a matrix that one or several of its columns have the maximum number of entries equal to zero. Thus, the minimum number of columns in X_b^{MP} satisfying the fault diagnosis equation (2.22) can be got. The corresponding partition (2.29) is called a canonical form of the fault diagnosis equation. Notice that according to fault verification principles [2] it is enough to find a single entry in one column of *C* equal to zero to solve the fault diagnosis equation. This column and all rows with non-zero entries will correspond to the faulty parameters indicated by the element of co-basis B_2 and elements of basis B_1, respectively.

In this dissertation, a numerically robust algorithm based on the *QR* factorization [19] will be referred to find a numerically stable solution of over determined system of linear equations that minimizes the least square error. Fault diagnosis equation uses more

measurements than the number of unknown variables in order to be able to find a unique solution as well as to compensate for the measurement errors and noise of the measurement equipment. At least one extra measurement is needed to verify the fault selection hypothesis. As a result of the QR factorization of $(m-1)xp$ verification matrix B, the following equation can be obtained:

$$BE = QR \tag{2.31}$$

where E is pxp column selection matrix, Q is $(m-1)x(m-1)$ orthogonal matrix, and R is $(m-1)xp$ upper triangular matrix. Each column of matrix E has only one nonzero entry, which is equal to one. Matrix product BE represents a permutation of the original columns of the verification matrix B. Matrix R has its rank equal to the rank of matrix B. Since R is an upper triangular matrix and $m-1<p$, R can be written as

$$R = \begin{bmatrix} R_1 & R_2 \\ 0 & 0 \end{bmatrix} \tag{2.32}$$

where R_1 is $r \times r$ upper triangular and has its rank equal to the rank of the verification matrix B.

The following theorem in [19] provides a basis for a numerically efficient approach to finding the ambiguity groups.

Theorem:

A linear combination matrix C can be numerically obtained from the QR factorization of the verification matrix B using

$$C = R_1^{-1} R_2 \tag{2.33}$$

2.3.2.3. Element Swapping

A single QR run cannot guarantee that the matrix C will be obtained with one or several of its columns having the maximum number of zero entries unless the proper basis is selected. To find a minimum form partition, it is necessary to swap one parameter of the basis with one parameter of the co-basis in the ambiguity cluster in order to increase the number of nonzero entries in C. Note that swapping parameters of the basis and the co-basis can be performed independently in different ambiguity clusters, since different clusters have mutually disjoint sets of parameters.

Lemma 1 [19]:

The necessary condition for swapping to increase the number of zero entries in C is that the columns of basis and co-basis to be swapped have a singular 2x2 sub-matrix of nonzero entries.

Let us consider a linear combination matrix C with a *2x2* singular sub-matrix $\begin{bmatrix} c_{jk} & c_{jm} \\ c_{ik} & c_{im} \end{bmatrix}$ with all nonzero entries. If the j^{th} element of the basis is swapped with k^{th} element of the co-basis, then after swapping, the k^{th} column of C changes to

$$C_k = -\frac{1}{c_{jk}}\begin{bmatrix} c_{1k} & c_{2k} & \cdots & 1 & \cdots & c_{rk} \end{bmatrix}^T \tag{2.34}$$

In addition, all other columns of matrix C will be equal to

$$C_n = \begin{bmatrix} c_{1n} - \frac{c_{jn}c_{1k}}{c_{ik}} & c_{2n} - \frac{c_{jn}c_{2k}}{c_{ik}} & \cdots & \frac{c_{jn}}{c_{ik}} & \cdots & c_{rn} - \frac{c_{jn}c_{rk}}{c_{ik}} \end{bmatrix}^T \tag{2.35}$$

such that all zero locations in the k^{th} column of C will remain zero as they were in the original C. However, as can be deducted from (2.34), a nonzero location c_{im} in row i and column m will become zero. Let us analyze this column m with at least one zero entry. The circuit parameter in the basis corresponding to such a column m is selected first, then the circuit parameters in the co-basis corresponding to all non-zero entries in column m are selected. An ambiguity group F is formed by combining the selected basis parameter with the co-basis parameters. Any column of C with zero entries form an ambiguity group F and has to be consider for further processing. Since ambiguities may exist in the original matrix X_b^{MP} then F contains all faults in the CUT only if the corresponding columns in X_b^{MP} are independent. Hence the following lemma can be formulated:

Lemma 2:

A necessary condition for an ambiguity group F of the linear combination matrix C to contain the set of all faults in the tested circuit is that the rank of the corresponding columns in matrix X_b^{MP} is equal to the cardinality of F.

$$rank(X_b^{MP}) = card(F) \tag{2.36}$$

Thus, according to Lemma 2, any ambiguity group of the verification matrix which do satisfy (2.36) needs to be verified.

The purpose of column swapping is to find out at least one ambiguity group of a minimum size. It is possible to locate several different ambiguity groups with minimum size and all of them will satisfy Lemma 2. The last step of fault location is to check

whether the sub-matrix of X_b^{MP} corresponding to such an ambiguity group can satisfy fault diagnosis equation or not. If yes, the circuit parameters corresponding to such a minimum size ambiguity group are concluded as a set of faulty parameters, F. Hence, the coefficient matrix X_b^{MF} is also determined.

The number of operations required for Gaussian elimination step is $O(p^2)$, $O(p^3)$ operations are needed for QR factorization and $O((p-r)^3)$ for column swapping, so the computational cost of the developed technique is $O(p^3)$. It is more efficient than comprehensive search whose number of operations is $O\left(\sum_1^f \binom{p}{i}\right)$.

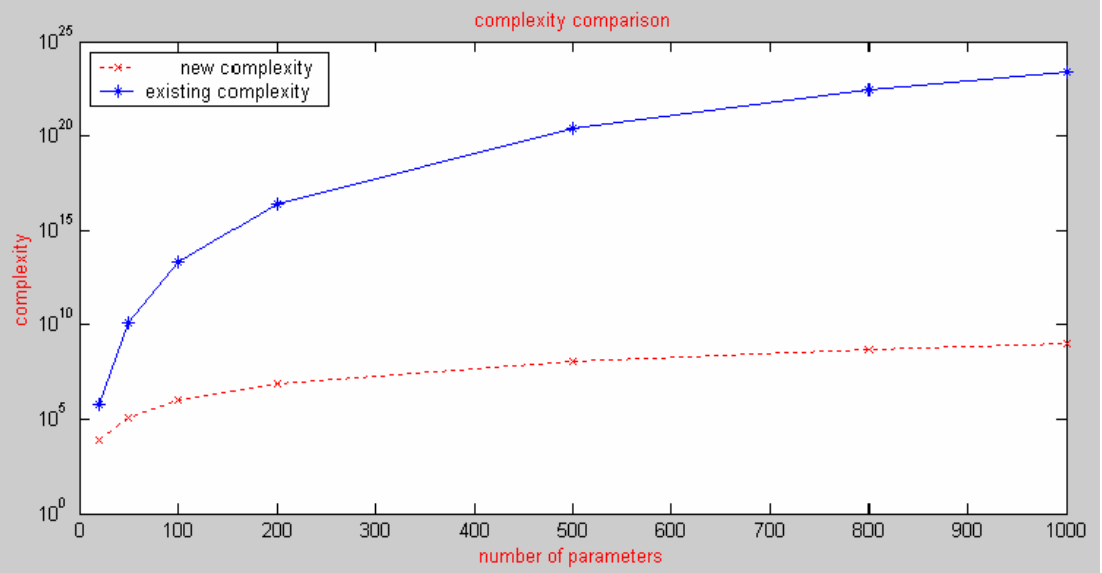

Figure 2.2 Complexity comparison: comprehensive search vs. ambiguity group locating

Fig. 2.2 illustrates the complexity comparison between comprehensive search and ambiguity group location technique. Suppose that the number of faults, *f*, is equal to 10,

the number of circuit parameters is 20, 50, 100, 200, 500, 800 and 1000 respectively. The ambiguity group locating technique requires fewer operations, especially when the number of parameters is large.

2.3.3. Parameter Evaluation

After location of the faulty parameters (and determination of X_b^{MF}), the invariant vector a_i can be uniquely solved from (2.22):

$$a_i = \left(\left(X_b^{MF} \right)^T X_b^{MF} \right)^{-1} \left(X_b^{MF} \right)^T \Delta X_i^M \qquad (2.37)$$

Then, the parameter deviation vector d can be exactly computed by

$$d = a_i \; rdivide \left(-b_i - a_i g \right) \qquad (2.38)$$

where *rdivide* is an element-by-element division of two vectors. Additionally, the other variables in the faulty circuit can be obtained from the construction process of fault diagnosis equation. For example, the entire deviation vector ΔX can be obtained by using (2.18) and considering (2.16). Then the solution vector for faulty circuit *X* can be obtained from (2.8). Alternatively, vector *X* can be solved from (2.6) by inverting its coefficient matrix *T*, obtained by (2.7) and (2.10). In one word, everything about the faulty circuit can be known.

2.3.4. Algorithm for Fault Diagnosis

A flow diagram of a computer program which implements the fault diagnosis discussed above is shown in Fig. 2.3. Since most of the phases of the algorithm are self-evident from the flow diagram, only some phases are detailed in this section.

In Phase 1, since nominal values of circuit parameters are known and all nodal voltages in fault-free circuit can be solved by (2.5), only the nodal voltages of the i^{th} node in the CUT under multiple excitation method is needed for measurement to obtain measurement deviation vector ΔX_i^M .

In Phase 5, F denotes one suspicious fault set and ***min(size(F))*** represents a scalar which is equal to the minimum size of all suspicious fault sets.

In Phase 6, if several suspicious fault sets have the same minimum size, ***min(size(F))***, select one of them arbitrarily for analysis. Only one parameter in the selected F is from the co-basis and the remaining parameters from the basis. Swap that co-basis parameter which corresponds to column k in matrix C with one of basis parameters which corresponds to row j in the matrix C. By (2.34) and (2.35), all zero entries in the column k of matrix C will be maintained after swapping while new zero-entry will appear in another column of new matrix C, thus the new value of ***min(size(F))*** will be equal to, or less than the old value before swapping.

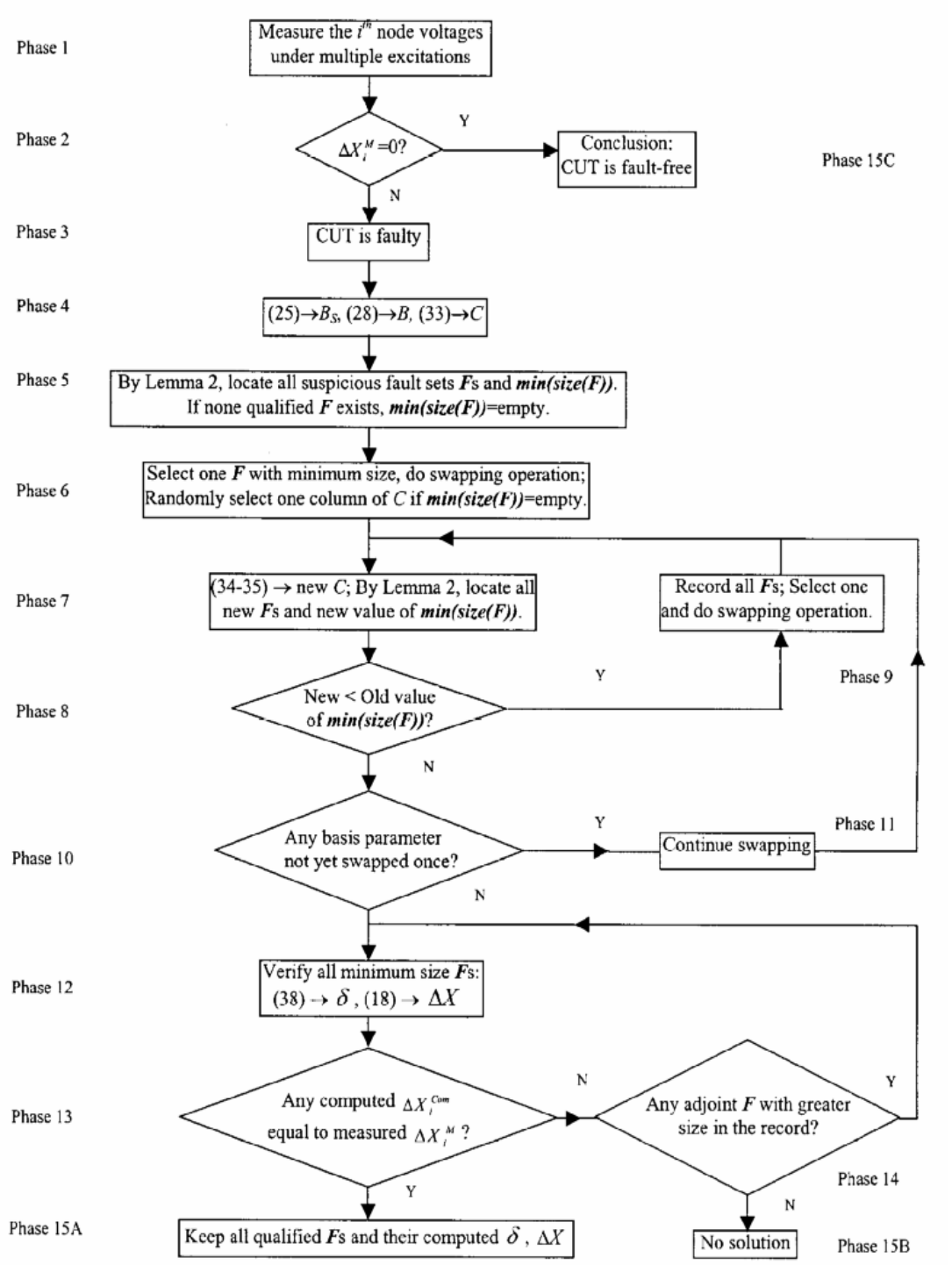

Figure 2.3 Algorithm for fault verification technique [39]

There are two rules for swapping. One is that, according to Lemma 1, row *j* is selected with nonzero c_{jk} on the intersection of row *j* and column *k* of matrix *C.* Another rule is that if one parameter in the current basis has been swapped into the basis by the previous swapping operation, then this element will not be considered during the later swapping operation. Usually *m-1* is far less than *p*, and the rank of *rx(p-r)* matrix *C*, *r* is not greater than *m-1*, thus there are far less basis parameters than co-basis parameters. The comprehensive swapping between the co-basis parameter *k* and the basis parameters are very limited, as a result of the two swapping principles.

Phases 12 through 15B are used for verification. One or several suspicious fault sets with minimum size are used to compute the deviation vector ΔX . If a computed vector matches the real measured vector ΔX_i^M , the corresponding fault set *F* is our final solution to faulty parameters. Otherwise, this set is discarded, and turn to the adjoint suspicious fault sets recorded in Phase 9. Verification in this phase continues until finding out at least one qualified solution to faulty parameters. Otherwise, the CUT is concluded as un-solvable because the restriction $f \le m-1$ discussed in Section 2.2 is not satisfied.

2.4. Example Circuits

Example 2.1: The example circuit 4 in [21] is used here (Fig. 2.4) in order to demonstrate the improvement in efficacy by the method proposed in this paper. There are 6+1 nodes, 11 conductances, 2 voltage-controlled-current sources in the CUT, where

G_1=1S, G_2=1S, G_3=2S, G_4=1S, G_5=0.5S, G_6=2S, G_7=1S, G_8=0.5S, G_9=2S, G_2=1S, G_{11}=0.5S, i_s=1A.

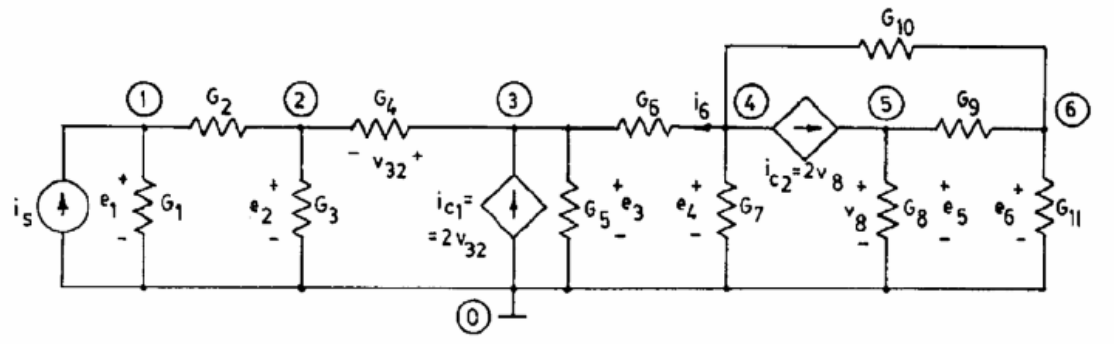

Figure 2.4 Example circuit in [21]

Suppose that G_3 and G_9 have deviations $\Delta G_3 = -1\ S$ and $\Delta G_9 = 2\ S$, respectively. Node *{1}* is the single measurement node. The single current source i_s is applied between ground and three accessible nodes *{1, 3, 6}* respectively under multiple excitation method. Thus, *n=6, p=13, m=3, f=2* and $f \le m-1 \le p$. The measurement deviation in Phase 1 of algorithm is

$$\Delta X_i^M = \begin{bmatrix} 0.2248 \\ -2.1536 \\ -1.2544 \end{bmatrix}$$

In Phase 4, verification matrix B is obtained after Gaussian elimination as

$$B = \begin{bmatrix} 5.3827 & -4.1975 & 1.1852 & -1.8272 & -0.6420 & 0.7531 & 0.1111 & -0.9877 & 0.7407 & -0.3580 & -0.2469 & 0.6420 & 1.0988 \\ 3.3827 & -2.1975 & 1.1852 & 0.1728 & 1.3580 & -0.2469 & 1.1111 & -0.9877 & 0.7407 & -1.3580 & -0.2469 & -1.3580 & 2.0988 \end{bmatrix}$$

and the linear combination matrix C is obtained as

$$C=\begin{bmatrix} 0.2500 & -0.2500 & -0.7500 & 0.0911 & 0.0911 & -0.2083 & 0.1563 & -0.1432 & -0.0521 & 0 & 0.2995 \\ 0.2500 & 0.7500 & 0.2500 & -0.4089 & 0.5911 & -0.2083 & 0.1562 & -0.6432 & -0.0521 & -1.0000 & 0.7995 \end{bmatrix}$$

with permutation vector *E={1, 5, 3, 4, 2, 6, 7, 8, 9, 10, 11, 12, 13}*. Thus the basis parameters are *{1, 5}* and co-basis parameters are *{3, 4, 2, 6, 7, 8, 9, 10, 11, 12, 13}*. There is only one column, the 10^{th} column of *C*, with zero entry. The corresponding ambiguity group (or suspicious fault set) is *{5, 12}*, but it does not satisfy Lemma 2.

Swapping the first basis parameter *{1}* with the first co-basis parameter *{3}*, the new matrix *C* is obtained as

$$C=\begin{bmatrix} 4.0000 & -1.0000 & -3.0000 & 0.3646 & 0.3646 & -0.8333 & 0.6250 & -0.5729 & -0.2083 & 0 & 1.1979 \\ -1.0000 & 1.0000 & 1.0000 & -0.5000 & 0.5000 & 0.0000 & -0.0000 & -0.5000 & 0.0000 & -1.0000 & 0.5000 \end{bmatrix}$$

Totally there are three suspicious fault sets *{3, 8}*, *{3, 9}* and *{3, 11}*, and ***min(size(F))***=2. Note that the suspicious fault set {5, 12} has already been excluded by Lemma 2 in former analysis. Since ***min(size(F))*** cannot been reduced any more by swapping, it is concluded that these three fault sets are our candidates for verification in Phase 13 through 15B.

For the fault set *{3, 8}*, the fault diagnosis equation is

$$\begin{bmatrix} 0.2248 \\ -2.1536 \\ -1.2544 \end{bmatrix} = \begin{bmatrix} -0.1304 & 0.6957 \\ 2.4348 & -7.6522 \\ 1.9130 & -4.8696 \end{bmatrix} a_i$$

with its unique solution vector by (2.37) $a_i = [0.3191 \quad 0.3830]^T$. By (2.38), the deviations of G_3 and G_8 are

$$\begin{bmatrix} \Delta G_3 \\ \Delta G_8 \end{bmatrix} = \begin{bmatrix} -1.0000 \\ 0.2647 \end{bmatrix}$$

The computed nodal voltage deviations on node *{1}* is

$$\Delta X_i^{computed} = \begin{bmatrix} 0.2248 \\ -2.1536 \\ -1.2544 \end{bmatrix}$$

which is equal to the measured vector ΔX_i^M . Thus, it is concluded that fault parameters are G_3 and G_8 with $\Delta G_3 = -1 \ S$ and $\Delta G_8 = 0.2647 \ S$ respectively.

For fault set *{3, 9}*, the fault diagnosis equation is

$$\begin{bmatrix} 0.2248 \\ -2.1536 \\ -1.2544 \end{bmatrix} = \begin{bmatrix} -0.1304 & -0.5217 \\ 2.4348 & 5.7391 \\ 1.9130 & 3.6522 \end{bmatrix} a_i$$

with the deviations of G_3 and G_9 are equal to

$$\begin{bmatrix} \Delta G_3 \\ \Delta G_9 \end{bmatrix} = \begin{bmatrix} -1.0000 \\ 2.0000 \end{bmatrix}$$

The computed vector of nodal voltage deviations on node *{1}* is also equal to the measured vector ΔX_i^M . It is concluded that fault parameters are G_3 and G_9 with $\Delta G_3 = -1 \ S$ and $\Delta G_9 = 2.0000 \ S$ respectively.

For fault set *{3, 11}*, similar conclusion is made that fault parameters are G_3 and G_{11} with $\Delta G_3 = -1\ S$ and $\Delta G_{11} = 1.6364\ S$ respectively.

Totally three solutions to the faulty parameters for the given measurements are obtained. To exactly identify the faulty parameters in the CUT, more measurements are needed, which will be demonstrated in next example.

The accessible nodes are reduced to 3 (nodes *1, 3,* and *6*) in the developed Woodbury fault verification technique comparing with at least 4 accessible nodes in [21]: nodes *{1, 6}* for multiple excitations and nodes *{3, 4}* for measurements of the branch voltages at G_6. The selection and assumption of one fault-free parameter with corresponding measurement of its branch voltage used in decomposition method in [21] is removed, which is a notable improvement.

Example 2.2: An active low-pass filter [37] is provided as one example to illustrate the approach described in Section 2.3. The example circuit has 20 nodes and 22 resistors, 4 capacitors, and 8 amplifiers with the following nominal values (all resistors in $k\Omega$ and capacitors in mF): R_1*=0.182,* C_2*=0.01,* R_3*=1.57,* R_5*=2.64,* R_6*=10.0,* R_7*=10.0,* R_9*=100.0,* R_{10}*=11.1,* R_{11}*=2.64,* C_{12}*=0.01,* R_{14}*=5.41,* R_{15}*=1.0,* R_{17}*=1.0,* C_{18}*=0.01,* R_{19}*=4.84,* R_{21}*=2.32,* R_{22}*=10.0,* R_{23}*=10.0,* R_{25}*=500.0,* R_{26}*=111.1,* R_{27}*=1.14,* R_{28}*=2.32,* C_{29}*=0.01,* R_{31}*=72.4,* R_{32}*=10.0,* R_{34}*=10.0*.* The current source is $j(t) = 1.0\cos(2000\,t)\,A$.

The filter is shown in Fig. 2.5 and all the operational amplifiers are modeled by the circuit in Fig. 2.6.

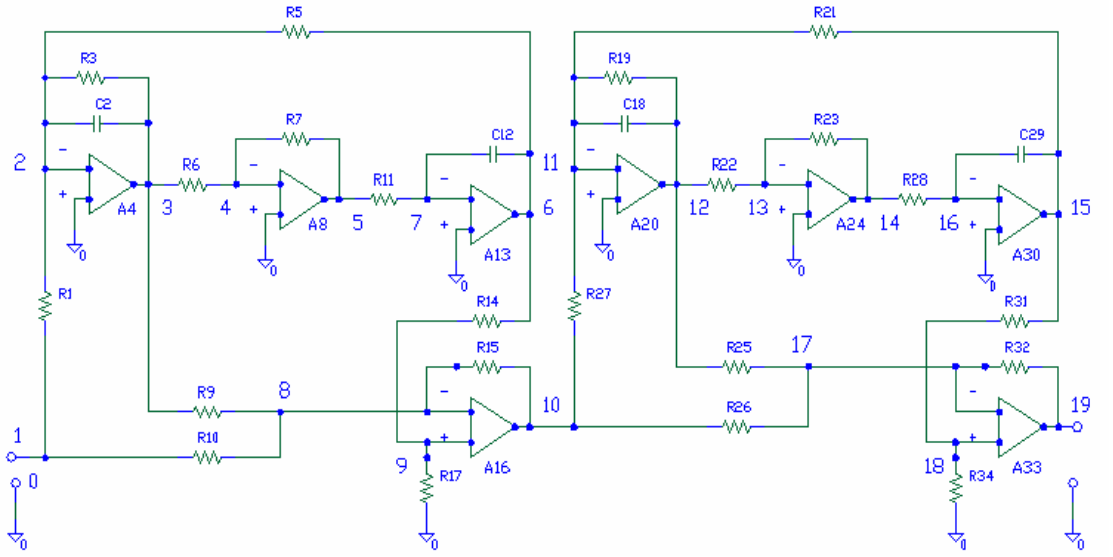

Figure 2.5 Active low pass analog filter

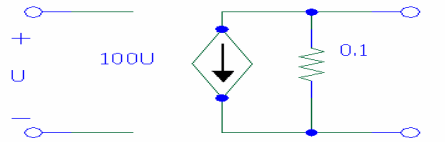

Figure 2.6 Model for operational amplifier

Assume that the faulty parameters are R_6 which was changed from 10.0 $k\Omega$ to 20.0 $k\Omega$ and R_{26} changed from 111.1 $k\Omega$ to 75.0 $k\Omega$. The corresponding admittance deviations are $\Delta G6 = 1/20000 - 1/10000 = -5.0 \times e^{-5}/\Omega$ and $\Delta G26 = 1/75000 - 1/111100 = 4.3324 \times e^{-6}/\Omega$. The single measurement node is node {*2*}, and the single current source is applied between ground and nodes {*1, 2, 7, 17, 19*}, respectively. Thus *n=19*,

p=42, *f=2*, *m=5* and the restriction $f \le m-1 \le p$ is satisfied. The measured deviation vector in Laplace domain is

$$\Delta X_i^M = \begin{bmatrix} -3.4938 \times e^{-3} + 1.3508 \times e^{-2} i \\ -3.5511 \times e^{-3} + 1.3729 \times e^{-2} i \\ 2.6940 \times e^{-1} + 7.0256 \times e^{-2} i \\ -5.1196 \times e^{-14} + 2.1975 \times e^{-13} i \\ -3.5511 \times e^{-3} + 1.3729 \times e^{-2} i \end{bmatrix}$$

In Phase 4, a *4x38* linear combination matrix *C* is obtained after Gaussian elimination and QR factorization with the basis parameters *{3, 30, 7, 17, 5}* and co-basis parameters *{6, 1, 8, 9, 10, 11, 12, 13, 14, 15, 16, 4, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42}*. By Lemma 2, two suspicious fault sets are identified *{5, 17}* and *{4, 17}* with ***min(size(F))****=2*.

Since no swapping can reduce ***min(size(F))*** any more, two suspicious fault sets *{5, 17}*, and *{4, 17}* are obtained.

Fault set *{4, 17}*, corresponds to parameters *{R6, R26}* in the CUT. The fault diagnosis equation is

$$\begin{bmatrix} -3.4938\times e^{-3} + 1.3508\times e^{-2} i \\ -3.5511\times e^{-3} + 1.3729\times e^{-2} i \\ 2.6940\times e^{-1} + 7.0256\times e^{-2} i \\ -5.1196\times e^{-14} + 2.1975\times e^{-13} i \\ -3.5511\times e^{-3} + 1.3729\times e^{-2} i \end{bmatrix} = \begin{bmatrix} -1.1044e^{+1} + 1.3172e^{+2} i & -5.5322e^{+2} - 4.9887e^{+1} i \\ -1.1225e^{+1} + 1.3388e^{+2} i & -5.4184e^{+2} - 5.0614e^{+1} i \\ 2.6279e^{+3} + 2.2562e^{+2} i & -9.4639e^{+2} - 5.6622e^{+1} i \\ -9.0468e^{-11} + 1.0790e^{-9} i & 1.0101e^{0} + 6.4128e^{-11} i \\ -1.1225e^{+1} + 1.3388e^{+2} i & -5.4183e^{+2} - 5.0614e^{+1} i \end{bmatrix} a_i$$

with $a_i = \begin{bmatrix} 1.0404 \times e^{-4} - 1.7802 \times e^{-5} i & -2.2349 \times e^{-14} - 1.0800 \times e^{-13} i \end{bmatrix}^T$. By (2.38), the deviations of G_6 and G_{26} are

$$\begin{bmatrix} \Delta G_6 \\ \Delta G_{26} \end{bmatrix} = \begin{bmatrix} -5.0000 \times e^{-5} + 6.3277 \times e^{-21} i \\ 4.3324 \times e^{-6} + 3.6403 \times e^{-12} i \end{bmatrix} \approx \begin{bmatrix} -5.0000 \times e^{-5} \\ 4.3324 \times e^{-6} \end{bmatrix}$$

The computed vector of nodal voltage deviations on node *{2}* is also equal to the measured vector ΔX_i^M . G_6 and G_{26} are concluded as the faulty parameters with $\Delta G_6 = -5 \times e^{-5}\ S$ and $\Delta G_{26} = 4.3324 \times e^{-6}\ S$.

Fault set *{5, 17}* corresponds to parameters *{R7, R26}* in the CUT. By (2.38), the deviations of G_7 and G_{26} are

$$\begin{bmatrix} \Delta G_7 \\ \Delta G_{26} \end{bmatrix} = \begin{bmatrix} 9.9075 \times e^{-5} - 1.5686 \times e^{-7} i \\ -7.7897 \times e^{-13} + 3.9789 \times e^{-12} i \end{bmatrix}$$

Obviously, R_7 should not have imaginary part even in the faulty condition. Thus, this fault set is discarded.

In conclusion, only one faulty parameter set *{R6, R26}* is identified with their deviations in the CUT, which is the exact faulty condition in the CUT. Thus by increasing the number of measurements, the suspicious faulty parameter sets are reduced to a unique solution set which matches the real condition.

2.5. Generalized Applications

Comparing with the research in [21], multiple excitations and Woodbury formula are also required for fault identification in my work [38-39]. A recently developed ambiguity group locating technique is modified and applied for fault identification which

reduces computational cost of test method. Multiple faults can be located directly and efficiently, thus eliminating the requirement for decomposition and the corresponding restrictions in [21].

The mechanism demonstrated in the described technique can be generalized as follows. First, construct the fault diagnosis equation based on circuit analysis and measurements to relate the limited measured circuit responses with the faulty parameters in a linear way, then apply the ambiguity group locating technique to identify the faulty parameters through three steps: Gaussian elimination, QR factorization and column swapping. Finally evaluate all parameter values of the faulty circuit based on the analysis of the fault diagnosis equation. Two new fault verification techniques sharing the same mechanism were proposed for multiple fault diagnosis in linear analog circuits. Simultaneously, an advanced technique to eliminate Gaussian elimination and column swapping in general ambiguity group locating technique is described at the end of this chapter to reduce more computation cost.

2.5.1. Nominal Fault Verification Technique

This technique is described in detail in [40]. It is called **nominal fault verification technique** in this dissertation, since its fault diagnosis equation uses the inverse of the nominal coefficient matrix. Starting from (2.5) and (2.6), following equation can be obtained

$$T_0 \, \Delta X = -\Delta T \; X \tag{2.39}$$

Then ΔX is computed by

$$\Delta X = -T_0^{-1}\,\Delta T\; X \tag{2.40}$$

Let us denote

$$\Delta W = -\Delta T\; X \tag{2.41}$$

where *gx1* vector ΔW represents the changes in excitations caused by faulty parameters. And it is called the **faulty excitations** in this dissertation. The corresponding nodes or parameters are faulty. Similarly, nodes or parameters with zero faulty excitations are fault-free. The equation (2.40) is simplified as

$$\Delta X = T_0^{-1}\,\Delta W \tag{2.42}$$

Since only a few parameters are faulty, in which case ΔW has the form

$$\Delta W = \begin{bmatrix} 0 \\ \Delta W^{F} \\ 0 \end{bmatrix} \tag{2.43}$$

Assuming that the first *m* elements of *X* can be measured, following equation is obtained

$$\begin{bmatrix} \Delta X^{M} \\ \Delta X^{G-M} \end{bmatrix} = T_0^{-1} \begin{bmatrix} 0 \\ \Delta W^{F} \\ 0 \end{bmatrix} \tag{2.44}$$

where *G* indicates the set of all equations, *M* the set of measurements. Hence, the nominal fault diagnosis equation is obtained as:

$$\Delta X^{M} = B_{MF}\;\Delta W^{F} \tag{2.45}$$

where

$$T^{-1} = \begin{bmatrix} B_{M1} & B_{MF} & B_{M2} \\ B_{N-M,1} & B_{N-M,F} & B_{N-M,2} \end{bmatrix} \tag{2.46}$$

$$B_M = \begin{bmatrix} B_{M1} & B_{MF} & B_{M2} \end{bmatrix} \tag{2.47}$$

So, the fault diagnosis matrix B_{MF} is a sub-matrix of the nominal coefficient matrix inverse.

The nominal fault diagnosis equation (2.45) has to be satisfied when the set F includes all circuit excitations associated with faulty parameters in the faulty circuit. The columns in B_{MF} correspond to faulty nodes or faulty parameters in the circuit. Our aim is to find out the sets of columns in matrix B_M that satisfy equation (2.45) with the minimum number of faults, that is, vector ΔW^F has the minimum number of nonzero values.

The same ambiguity group locating technique discussed in Section 2.3.2 can be applied to identify the minimum form ambiguity group after constructing a *mx(g+1)* matrix B_s as follows.

$$B_S = [\Delta X^M \quad B_M] \tag{2.48}$$

After location of faulty excitations, the deviation of the faulty excitation vector can be derived by solving (2.45),

$$\Delta W^F = \left(B_{MF}{}^T B_{MF}\right)^{-1} B_{MF}{}^T \Delta X^M \tag{2.49}$$

Then, the deviation of the excitation vector can be obtained by filling out the remaining elements with zeros to get ΔW in (2.43). The deviation of the solution vector ΔX can be obtained by (2.42), and the solution vector for faulty circuit X can be obtained by (2.8). Combining (2.10) into (2.41),

$$\Delta W = -\Delta T\, X = -P_f\, diag(d)\, Q_f^T\, X = X_{inc}\, d \tag{2.50}$$

where

$$X_{inc} = -P_f \; diag\,(Q_f^T X) \tag{2.51}$$

Assuming that k of p parameters are faulty and the resulting f of g excitations are faulty, k is no greater than f because some parameters may be located between two ungrounded nodes. Re-arrange the equation (2.50) as follows:

$$X_{inc}^{\,f,k}\; d^k + X_{inc}^{\,f,p-k}\, 0^{p-k} = (\Delta W)^f \tag{2.52a}$$

$$X_{inc}^{\,n-f,k}\; d^k + X_{inc}^{\,n-f,\,p-k}\; 0^{p-k} = 0^{n-f} \tag{2.52b}$$

Here the superscript indicates the size of the matrix or vector. The equation (2.52b) is worth consideration. Obviously with nonzero values of d^k, $X_{inc}^{\,n-f,k}$ must be $0^{n-f,k}$ with probability equal to 1. The position of faulty elements d^k can be obtained from the solution of equation (2.52b) as follows:

Lemma 3:

The k faulty parameters are included in the parameter set whose corresponding columns have all zero entries in the matrix $X_{inc}^{\,n-f,\,p}$.

The deviations of faulty parameters then can be derived by solving (2.52a)

$$d = \left(\left(X_{inc}^{\,f,k} \right)^T X_{inc}^{\,f.k} \right)^{-1} (X_{inc}^{\,f,k})^T \; (\Delta W)^f \tag{2.53}$$

2.5.2. Adjoint Fault Verification Technique

This technique is discussed in details in [41]. Similar as in the technique described in this chapter, but without Woodbury formula, combining (2.10) into (2.6), following equation is resulted

$$\left(T_0 + P_f \; diag\,(d)\, Q_f^T\right)\left(X_0 + \Delta X\right) = W_0 \tag{2.54}$$

After substituting (2.5) into (2.54), the following equation is established,

$$\Delta X = -\,T_0^{-1}\, P_f \;\; diag\;(d)\, Q_f^T\, X \tag{2.55}$$

Let us denote a *gxg* matrix S_0 as follows

$$S_0 = [s_1 \;\; s_2 \;\; \ldots \;\; s_g] = -T_0^{-1} \tag{2.56}$$

where X and $s_v\,(v = 1, 2, \ldots, g)$ are *gx1* vectors. Thus the products of S_0 and P_f, Q_f^T and X can be written as

$$\begin{aligned} S_{GF} &= S_0 P_f = S_0[e_{i_1} - e_{j_1} \;\; e_{i_2} - e_{j_2} \;\; \ldots \; e_{i_f} - e_{j_f}] \\ &= [s_{i_1} - s_{j_1} \;\; s_{i_2} - s_{j_2} \;\; \ldots \;\; s_{i_f} - s_{j_f}] \\ Q_f^T X &= [e_{k_1} - e_{l_1} \;\; e_{k_2} - e_{l_2} \;\; \ldots \; e_{k_f} - e_{l_f}]^T \; X \\ &= [x_{k_1} - x_{l_1} \;\; x_{k_2} - x_{l_2} \;\; \ldots \; x_{k_f} - x_{l_f}]^T \end{aligned} \tag{2.57}$$

where G indicates the set of all modified nodal equations and the **fault set** F represents the set of all the faulty parameters.

Denote an *fx1* vector

$$l_F = diag\,(d)\; Q_f^T X \tag{2.58}$$

and consider (2.9) and (2.57) to get

$$\begin{aligned} l_F &= diag\ (d)\ Q_f^T X \\ &= diag\ (d)\,[x_{k_1} - x_{l_1}\ \ x_{k_2} - x_{l_2}\ \ \ldots\ \ x_{k_f} - x_{l_f}]^T \\ &= [d_1(x_{k_1} - x_{l_1})\ \ d_2(x_{k_2} - x_{l_2})\ \ \ldots\ \ d_f(x_{k_f} - x_{l_f})]^T \end{aligned} \tag{2.59}$$

Thus (2.55) can be re-written as

$$\Delta X = S_{GF}\ l_F \tag{2.60}$$

Assume that the first m elements of ΔX can be measured and $f \le m-1 \le p$, following equation is resulted

$$\begin{bmatrix} \Delta X^{\ M} \\ \Delta X^{\ G-M} \end{bmatrix} = \begin{bmatrix} S_{MF} \\ S_{G-M,F} \end{bmatrix} l_F \tag{2.61}$$

where M represents the set of measurements. Hence, following **fault diagnosis equation** is obtained:

$$\Delta X^{M} = S_{MF}\ l_F \tag{2.62}$$

Here the fault diagnosis matrix S_{MF} is an *mxf* matrix whose columns correspond to the faulty parameters in the circuit. Similarly S_{MP} is an *mxp* matrix whose columns correspond to all of the parameters in the circuit, which is constructed by selecting all the rows corresponding to measurements selected from the following matrix S_{GP},

$$\begin{aligned} S_{GP} &= S_0 P = S_0[e_{i_1} - e_{j_1}\ \ e_{i_2} - e_{j_2}\ \ \ldots\ e_{i_p} - e_{j_p}] \\ &= [s_{i_1} - s_{j_1}\ \ s_{i_2} - s_{j_2}\ \ \ldots\ \ s_{i_p} - s_{j_p}] \end{aligned} \tag{2.63}$$

Notice that the elements of each column of the fault diagnosis matrix are the transfer functions from the location of a faulty element to all system nodes, or solutions

of the adjoint system with the output set at the location of the faulty element. For this reason, this technique is called adjoint fault verification technique.

Construct a *mx(p+1)* matrix B_S as follows,

$$B_S = [\Delta X^M \quad S_{MP}] \tag{2.64}$$

Then apply the ambiguity group locating technique from Section 2.3.2 to identify the minimum form ambiguity group. After location of ambiguity groups in fault diagnosis equation, it is known which parameters in the CUT are faulty. Vector l_F is then obtained by solving (2.62):

$$l_F = \left(S_{MF}{}^T S_{MF}\right)^{-1} S_{MF}{}^T \Delta X^M \tag{2.65}$$

The full vector ΔX can be computed by (2.60), since matrix S_{GF} and vector l_F are known now. The solution vector X is consequently determined by (2.8). Finally the parameter deviations d can be obtained by solving (2.59):

$$d = \left[\frac{l_1}{x_{k_1} - x_{l_1}} \quad \frac{l_2}{x_{k_2} - x_{l_2}} \quad \cdots \quad \frac{l_f}{x_{k_f} - x_{k_f}} \right]^T \tag{2.66}$$

2.5.3. Tableau Fault Verification Technique

Another fault verification technique developed in [42] is based on both multiple-excitation and multiple-measurement for the purpose of utilizing limited test accessibility to its full extend. The most significant highlight for this technique is that Gaussian elimination and swapping operations required by former verification techniques are eliminated, thus computational cost is further reduced.

There is a difference in circuit assumption: CUT has *n+1* nodes and *p* parameters in the impedance form Z_v $(v = 1, 2, \ldots, p)$. Such a circuit parameter Z_v can still be described by two-port like model in Fig. 2.1.

Suppose that there are *e* different excitations to the fault-free and faulty circuits. Apply KCL to fault-free circuit:

$$PI_{b0} = J \tag{2.67}$$

where I_{b0} is a *pxe* matrix of branch currents and J is a *nxe* matrix of independent branch current excitations (i.e. current sources located at individual parameters positions).

Apply Kirchhoff voltage law to the fault-free circuit:

$$Q^T V_{n0} - ZI_{b0} = 0 \tag{2.68}$$

where V_{n0} is a *nxe* matrix of nodal voltages which correspond to independent current excitations at all accessible nodes, Z is a *pxp* diagonal matrix of nominal parameter impedances:

$$Z=diag(Z_v) \tag{2.69}$$

Combining (2.67) and (2.68), following equation is resulted

$$\begin{bmatrix} 0 & P \\ Q^T & -Z \end{bmatrix} \begin{bmatrix} V_{n0} \\ I_{b0} \end{bmatrix} = \begin{bmatrix} J \\ 0 \end{bmatrix} \tag{2.70}$$

Assume that there are *f* of *p* faulty parameters in the faulty circuit with $f \leq e$. Correspondingly, the equation for the faulty circuit is as follows:

$$\left(\begin{bmatrix} 0 & P \\ Q^T & -Z \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & \Delta Z \end{bmatrix} \right) \left(\begin{bmatrix} V_{n0} \\ I_{b0} \end{bmatrix} + \begin{bmatrix} \Delta V_n \\ \Delta I_b \end{bmatrix} \right) = \begin{bmatrix} J \\ 0 \end{bmatrix} \tag{2.71}$$

where ΔZ is a *pxp* diagonal matrix of parameter deviations, ΔV_n is a *nxe* matrix of nodal voltage deviations, and ΔI_b is a *pxe* matrix of branch current deviations.

Denote

$$\begin{bmatrix} V_n \\ I_b \end{bmatrix} = \begin{bmatrix} V_{n0} \\ I_{b0} \end{bmatrix} + \begin{bmatrix} \Delta V_n \\ \Delta I_b \end{bmatrix} \tag{2.72}$$

Equation (2.71) can be simplified after considering (2.70):

$$\begin{bmatrix} 0 & P \\ Q^T & -Z \end{bmatrix} \begin{bmatrix} \Delta V_n \\ \Delta I_b \end{bmatrix} = \begin{bmatrix} 0 \\ -\Delta Z\, I_b \end{bmatrix} \tag{2.73}$$

Suppose that *m* nodal voltages are measured with *e*<*m*, then (2.73) can be decomposed as follows:

$$\begin{bmatrix} 0 & 0 & P \\ Q_1^T & Q_2^T & -Z \end{bmatrix} \begin{bmatrix} \Delta V_n^{\,M} \\ \Delta V_n^{N-M} \\ \Delta I_b \end{bmatrix} = \begin{bmatrix} 0 \\ -\Delta Z\, I_b \end{bmatrix} \tag{2.74}$$

where Q_1 is a *nxm* matrix and Q_2 is a *nx(p-m)* matrix.

Move the measured part to the right of (2.74) to obtain following form:

$$\begin{bmatrix} 0 & P \\ Q_2^T & -Z \end{bmatrix} \begin{bmatrix} \Delta V_n^{N-M} \\ \Delta I_b \end{bmatrix} = \begin{bmatrix} 0 \\ -\Delta Z\, I_b \end{bmatrix} + \begin{bmatrix} 0 \\ -Q_1^T\, \Delta V_n^{\,M} \end{bmatrix} \tag{2.75}$$

Fault diagnosis equation (2.75) relates the measured responses deviations $\Delta V_n^{\,M}$ with faulty parameter deviations ΔZ. The left-hand side *(n+p)x(n+p-m)* coefficient matrix of (2.75) can be constructed from the circuit topology and nominal values of circuit parameters. The solution matrix of (2.75) has a size of *(n+p-m)xe*. The right side of (2.75) is a *(n+p)xe* matrix with *fxe* unknow entries due to faulty parameters. Thus, *(n+p-*

f)xe linear equations with *(n+p-m)xe* variables can be obtained from (2.75). Since $m>f$, solution to (2.75) can be uniquely determined.

Construct a *(n+p+e-m)x(n+p)* new matrix by appending the coefficient matrix of (2.75) to the second item of the right side of (2.75):

$$B_S = \begin{bmatrix} 0 & 0 & P \\ -Q_1^T \Delta V_n^M & Q_2^T & -Z \end{bmatrix}^T \tag{2.76}$$

The columns of matrix B_S correspond to the combination of circuit nodes and parameters.

Now execute QR factorization described in Section 2.3.2.2 which results in a linear combination matrix *C*. Notice that there is no Gaussian elimination here, so the QR factorization is carrying out on verification matrix *B* in Woodbury verification technique (Section 2.3.2.2) while it is carrying out on matrix B_S here.

Fault diagnosis equation (2.75) is a very unusual equation. It contains unknown matrix of voltage and current deviations on the left-hand side and partly unknown right-hand side. The matrix B_S has the rank equal to *n+p+e-m* (where $f \le e < m$), however, the rank of

$$S = \begin{bmatrix} 0 & P \\ Q_2^T & -Z \end{bmatrix}$$

is equal to *n+p-m*. So, the increase in the rank of matrix B_S over the rank of matrix *S* is *(n+p+e-m)-(n+p-m)=e*. This rank increase is due to the presence of faulty parameters, which make part of the right-hand side of (2.75) independent on rows of matrix *S*. Therefore, all columns of matrix B_S which correspond to faulty parameters will be forced to the basis and (very important!) rows of matrix *S* which are not in the basis will be independent from these columns. This independency relation must be reflected in linear

combination matrix C by a row with all zero entries! Hence the following Lemma is resulted:

Lemma 4:

If all of the faulty parameters are included in the basis, then the circuit parameters corresponding to zero rows in the linear combination matrix C are faulty.

Since $f \le e$ and faulty parameters are independent from each other, all of the faulty parameters are guaranteed to be included in the basis. Therefore by applying Lemma 4 to linear combination matrix C, the faulty elements can be identified directly (No search for minimum size ambiguity group by column swapping at all!). In fact, the rows of linear combination matrix C are corresponding to a combination of circuit parameters and nodes. Some nodes associated with faulty excitations defined in Section 2.5.1 will be reflected in linear combination matrix C and may be located by Lemma 4. Tableau verification technique is to directly locate faulty parameters, so that these identified faulty excitation nodes could be used for verification or just discard them.

After location of faulty parameters, (2.75) can be decomposed according to positions of faulty parameters:

$$\begin{bmatrix} 0 & P \\ Q_{21}^T & -Z_{ff} \\ Q_{22}^T & -Z_f \end{bmatrix} \begin{bmatrix} \Delta V_n^{N-M} \\ \Delta I_b \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -\Delta Z_f I_b \end{bmatrix} + \begin{bmatrix} 0 \\ -Q_{11}^T \Delta V_n^M \\ -Q_{12}^T \Delta V_n^M \end{bmatrix} \quad (2.77)$$

or

$$\begin{bmatrix} 0 & P \\ Q_{21}^T & -Z_{ff} \end{bmatrix} \begin{bmatrix} \Delta V_n^{N-M} \\ \Delta I_b \end{bmatrix} = \begin{bmatrix} 0 \\ -Q_{11}^T \Delta V_n^M \end{bmatrix} \quad (2.78)$$

and

$$\begin{bmatrix} Q_{22}^T & -Z_f \end{bmatrix} \begin{bmatrix} \Delta V_n^{N-M} \\ \Delta I_b \end{bmatrix} = \begin{bmatrix} -\Delta Z_f \; I_b \end{bmatrix} + \begin{bmatrix} -Q_{12}^T \Delta V_n{}^M \end{bmatrix} \qquad (2.79)$$

Here the matrices Q_1, Q_2, Z, and ΔZ are decomposed into two parts: the first part corresponds to fault-free parameters, while the second one corresponds to faulty parameters.

The solution to (2.78) can be uniquely determined by

$$\begin{bmatrix} \Delta V_n^{N-M} \\ \Delta I_b \end{bmatrix} = \left((S_1)^t S_1 \right)^{-1} (S_1)^t \begin{bmatrix} 0 \\ -Q_{11}^T \Delta V_n{}^M \end{bmatrix} \qquad (2.80)$$

where $$S_1 = \begin{bmatrix} 0 & P \\ Q_{21}^T & -Z_{ff} \end{bmatrix}$$

Then, the values of branch currents in faulty circuit I_b can be obtained by (2.72). Re-arranging (2.79)

$$\Delta Z_f \; I_b = -\left(\begin{bmatrix} Q_{22}^T & -Z_f \end{bmatrix} \begin{bmatrix} \Delta V_n^{N-M} \\ \Delta I_b \end{bmatrix} + \begin{bmatrix} Q_{12}^T \; \Delta V_n{}^M \end{bmatrix} \right) = S_2 \qquad (2.81)$$

To reduce the computational efforts, one may select only one column I_{b1} from matrix I_b and only one column S_{21} from matrix S_2. The faulty parameter deviations can be exactly computed by solving (2.81):

$$\Delta Z_f = S_{21} \; rdivide \; I_{b1} \qquad (2.82)$$

where *rdivide* is an element-by-element division performance of two vectors. As an alternative, and to reduce effects of round-off errors, equation (2.81) could be solved by dividing S_2 by I_b element by element and taking row average to obtain ΔZ_f.

Comparing with the other verification techniques described in this chapter, tableau verification technique locates faulty parameters directly without Gaussian elimination step and without swapping operations, thus reducing the computational cost.

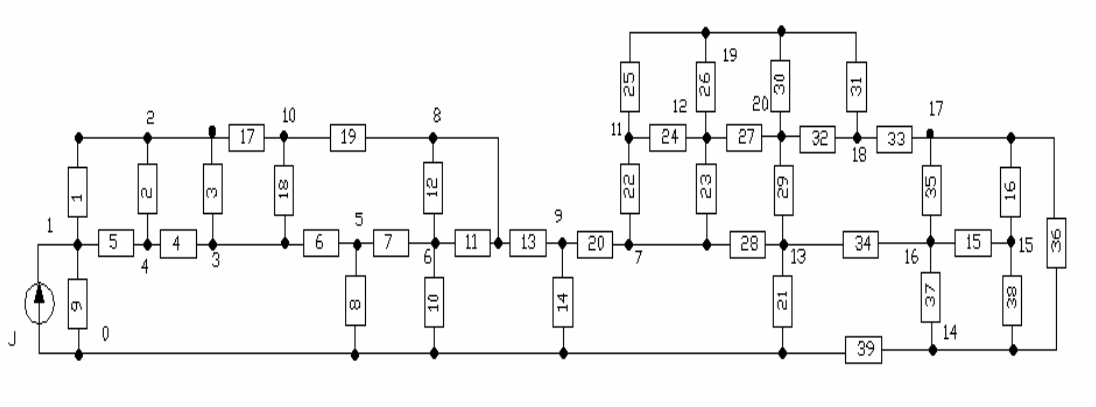

Figure 2.7 Resistive network example

Example circuit 2.3: The circuit shown in Fig. 2.7 with 21 nodes and 39 resistors is used to demonstrate the advanced verification technique. Nominal values of circuit parameters are as follows (all resistors in Ω):

$R_1=2.125$, $R_2=3.6$, $R_3=4.7$, $R_4=11.5$, $R_5=12.6$, $R_6=21.2$, $R_7=3.7$, $R_8=0.54$, $R_9=3.54$, $R_{10}=3.125$, $R_{11}=6.6$, $R_{12}=5.7$, $R_{13}=19.5$, $R_{14}=12.8$, $R_{15}=12.2$, $R_{16}=3.2$, $R_{17}=1.54$, $R_{18}=8.7$, $R_{19}=2.27$, $R_{20}=3.16$, $R_{21}=41.7$, $R_{22}=31.5$, $R_{23}=22.6$, $R_{24}=51.2$, $R_{25}=13.7$, $R_{26}=3.44$, $R_{27}=13.4$, $R_{28}=31.9$, $R_{29}=16.1$, $R_{30}=11.7$, $R_{31}=11.5$, $R_{32}=17.8$, $R_{33}=22.2$, $R_{34}=23.2$, $R_{35}=11.4$, $R_{36}=18.7$, $R_{37}=3.12$, $R_{38}=33.2$, $R_{39}=8.67$. The current source $J=1A$ is applied to nodes $\{0, 2\}$, $\{0, 16\}$ respectively. Note that current source is applied to nodes $\{0, 1\}$ in Fig. 2.6.

Assume that there are two faulty parameters: R_9 is changed from $3.54\,\Omega$ to $7.9\,\Omega$ and R_{37} is changed from $3.12\,\Omega$ to $2.8\,\Omega$. The corresponding impedance deviations are $\Delta Z9 = 4.36\ \Omega$ and $\Delta Z37 = -0.32\ \Omega$. The nodal voltages at nodes {*2, 4, 15, 16, 17*} are measured. Thus *n=20, p=39, e=2, f=2, m=5* and $f \le e < m$. The measured changes of nodal voltage under two distinct excitations are:

$$\Delta V_n^{\,M} = \begin{bmatrix} 8.9005 \times e^{-1} & 3.2306 \times e^{-2} \\ 9.1400 \times e^{-1} & 3.3316 \times e^{-2} \\ 3.6510 \times e^{-2} & -7.6708 \times e^{-2} \\ 3.2306 \times e^{-2} & -1.3351 \times e^{-1} \\ 3.8445 \times e^{-2} & -7.2593 \times e^{-2} \end{bmatrix}$$

which indicates the fault(s) detected inside the circuit.

Apply the QR factorization to the fault diagnosis equation. A *56x3* matrix *C* is obtained with rank of *r=56*. By analyzing permutation matrix *E*, co-basis includes only three circuit nodes {*4, 15, 17*} and the remaining 17 nodes and 39 parameters are included in the basis.

Analyzing *56x3* matrix *C*, three zero rows are found which correspond to parameters {*9, 37*} and node {*1*} respectively. According to Lemma 4, since all the circuit parameters are included in the basis, parameters {*9, 37*} are concluded as faulty parameters which are the exact solution for the given circuit. In fact, node {*1*} is a node associated with faulty excitatio ns defined in Section 2.5.1. It verifies that parameter {9} is faulty.

The deviations of nodal voltages and branch currents can be obtained by (2.80). The branch currents and the nodal voltages in the faulty circuit can be obtained by (2.72). Finally, the deviations of faulty parameters are exactly evaluated using (2.82):

$$\begin{bmatrix} \Delta Z_9 \\ \Delta Z_{37} \end{bmatrix} = \begin{bmatrix} 4.3600 \\ -0.3200 \end{bmatrix}$$

which are the exact deviation values of the faulty elements R_9 and R_{37}.

2.5.4. Comparisons of Four Fault Verification Techniques

Table 2.1 Comparison among four verification techniques

	Faulty Parameter Identification	**Excitation**	**Voltage Measurement**	**Circuit Analysis**	**Gaussian Elimination & Swapping**
Woodbury Verification	direct	multiple	single	Woodbury & modified nodal	yes
Nominal Verification	indirect	single	multiple	faulty excitations & modified nodal	yes
Adjoint Verification	direct	single	multiple	adjoint analysis	yes
Tableau Verification	direct	multiple	multiple	tableau analysis	no

The dominant feature of these four techniques is that all of them share the same mechanism discussed in Section 2.5. The differences among the techniques are in fault parameter location, circuit analysis tools, excitations, and measurements methods and are given in Table 2.1. Distinct fault diagnosis equations are constructed. As a consequence, distinct parameter evaluations are designed for each technique. There is no need for

Gaussian elimination and swapping operations for tableau verification technique comparing with other three verification techniques. All of these techniques belong to the same category of multiple fault verification in dynamic analog circuits and all of them benefit from efficient ambiguity groups location technique.

2.6. Conclusions

In this chapter, a generalized fault verification technique for dynamic analog circuits was discussed to accurately calculate faulty parameter deviations to address the ambiguity problem caused by limited measurements, and the intend of fault verification techniques is to obtain the information about the faulty circuit based on the limited measured responses of faulty circuit. There are two easily implemented prerequisites: one is that circuit topology and nominal values of circuit parameters should be known, another is that the number of measurements is greater than the number of faulty parameters. A new technique in this chapter is used to detect, and locate the multiple faults in a linear analog circuit in frequency domain, then to exactly calculate the faulty parameter deviations. For instance, applying the Woodbury formula to the modified nodal analysis, fault diagnosis equation is constructed to establish the relationship between the measured responses and the faulty parameter deviations in a linear way. Recently developed numerically robust approach for location of the minimum size ambiguity groups has been modified to fit in this chapter's condition to implement fault location. Specifically a fault diagnosis equation is analyzed using QR factorization and

possibly column swapping. Parameter evaluation is then performed using results of analysis of the fault diagnosis equation.

One node for voltage measurement is sufficient for the developed technique, although multiple excitations are required for fault location. Although faulty parameter deviation cannot be infinity, open or short condition can be dealt with well by switches in modified nodal analysis. Therefore, the faults can be parametric or catastrophic. The developed technique is extremely effective for large parameter deviations and a very limited number of accessible nodes used for excitations and measurements. The computation cost for fault location is on the order of $O(p^3)$, and compares favorably with the combinatorial search traditionally used in fault verification techniques which requires the number of operations $O\left(\sum_{1}^{f}\binom{p}{i}\right)$. A single fault diagnosis technique recently reported in [21] can be seen as a special case of the developed technique. Example circuits are used to illustrate the developed technique and improvement in the efficacy as compared with [21] is evident. Additionally, two new techniques for multiple fault diagnosis based on the same methodology are discussed. Finally, an advanced tableau verification technique is described to eliminate the requirements for Gaussian elimination and swapping operations by using multiple-excitation and multiple-measurement. The dominant differences among these techniques are the distinct fault diagnosis equations resulting from distinct circuit analysis methods and distinct excitation and measurement methods.

The technique described in this chapter can be classified under the category of Simulation-after-Test (SAT) [2], which can provide the exact solution to circuit

parameters and can be applied to detect large parameter changes when the number of independent measurements are greater than the number of faults in the CUT. It is very effective for limited accessibility cases.

CHAPTER 3 LARGE SCALE SYSTEM DECOMPOSITION

3.1. Complexity, Accessibility and Decomposition

Increased complexity and reduced accessibility are the most apparent in large scale mixed-signal systems and SoC products. Traditionally, testing of mixed-signal system and SoCs adopt the decomposition technique to partition the whole system into mechanical, software, analog, and digital subsystems in order to apply their domain specific test techniques. Finally system level test and interconnection test are applied to fulfill the testing task for the whole system. Among these subsystem testings, analog testing is the bottleneck as stated in Chapter 1. To address the practical problem of increasing scale of today's analog systems, design verification based on decomposition technique is the best candidate for verification of large-scale analog systems. Analog system decomposition was comprehensively explored in the 1980s by Bandler [43-44] to facilitate large scale analog test and fault diagnosis when computer resources were limited. With the astounding development of computation resources such as CPU and memory since the 1980s, research interests on analog decomposition diminished because it was not necessary to use decomposition in analog test and fault diagnosis. So that it is not surprising to see that there is limited literature on analog fault diagnosis by decomposition [22-23, 45, 46] although the idea of decomposition gained widespread application in test-related areas such as in test generation [24], fault model [47] and neural network-based fault diagnosis [48]. The most dominant approach in fault diagnosis was to combine decomposition technique with other test techniques, that is, first

decompose large scale system into smaller pieces and then to apply other techniques to test those subsystems.

The most promising advantage of the decomposition technique is that there is no upper bound to the number of faulty components in the system unlike in verification techniques. Another advantage is to reduce the test cost for large scale system because of one important fact: only very limited number of faults occurs in practice. After decomposition, fault-free subsystems usually occupy a large portion of the complete system. Therefore the entire testing effort can be devoted to the faulty subsystems.

In [22], decomposition approach was combined with modeling approach for board-level fault identification. After decomposition, regression models of the decomposed subsystems are tested. However, hundreds of circuit simulations are required to complete the fault diagnosis. Another decomposition method made use of the self-test algorithm and the component-connection model [23]. The so-called hierarchical components have to be determined before fault diagnosis. Hence, fault coverage is limited because not all circuit components are defined as hierarchical components. In decomposition method described in [43-44], faults are localized to within the smallest possible subsystems according to hierarchical decomposition structure. The current consistency of internal nodes is checked to locate faults. Based on work in [43-44], a method was designed in [45] to identify faulty subsystems under a nodal decomposition strategy. It is based on checking the voltage consistency of internal nodes in analyzed subsystems. Another decomposition approach was derived from [43-44] and presented in [46] to apply decomposition approach for parameter identification techniques [2]. All methods in [43-46] have a strict requirement: all decomposition nodes have to be

accessible to measurement. Thus, many accessible nodes are needed in order to locate faulty components or faulty regions within the small subsystems. Simultaneously, the fact that only accessible nodes could be the decomposition nodes restricts decomposition flexibility. Such requirement is not acceptable for today's analog networks whose scale is steadily increasing while the accessibility of the network nodes is decreasing. To achieve more information about the faulty components or faulty regions, there must be a compromise between the number of accessible nodes and the subsystems size.

A new technique is developed in this chapter [49] to alleviate this problem in order to face up to today's practice. Traditional decomposition technique is generalized to include subsystems not explicitly testable. Based on the network topology and checking consistency of KCL equations, nodal voltages of some specific inaccessible nodes under faulty conditions could be computed. Hence, these computed nodal voltages can be treated as measurements and subsequently be used for decomposition. For analog systems with sufficient accessibility, this technique can reduce the measurement cost. For analog systems with limited accessibility, this technique can create more decomposition nodes and can increase decomposition flexibility. This generalized decomposition can be applied to linear or non-linear systems. In Section 3.2, restriction on decomposition nodes is removed by selecting some specific inaccessible nodes based on location of fault-free systems and location of faulty subsystems. An efficient solution to location of fault-free nodes and verification of decomposed subsystems is also provided in Section 3.3 as one of choices when testing faulty subsystems. It is based on QR factorization technique for finding ambiguity groups and solving ambiguous equations. An example circuit is

provided in Section 3.4 to illustrate the efficiency of the developed technique. In Section 3.5, a summary is given.

3.2. Location of Fault-Free Subsystems and Faulty Subsystems

There are two assumptions for the generalized decomposition. The first one is that network topology and nominal values of network parameters are known, thus all the nodal voltages, branch currents and parameters information are known before testing and such computations can be carried out off-line. The second one is that all of the partitioned subsystems should be mutual coupling free. Let us begin with an important assumption used by decomposition technique presented in [43] which will be alleviated by the generalized decomposition in this chapter: **all the decomposition nodes should be accessible to voltage measurements**. For the system-under-test, some subsystems are fault-free, some are faulty. It is easier to locate fault-free subsystems than faulty subsystems according to Lemma 1-3 in [43]. The first step of generalized decomposition is to locate as many as possible fault-free subsystems based on the following corollary which is derived from Lemma 2 in [43]. Fig. 3.1 is the illustration of a common code. In

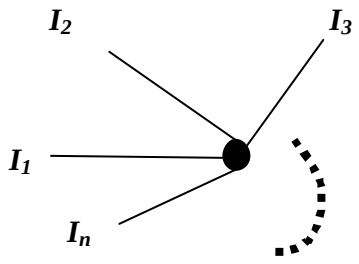

Figure 3.1 Illustration of a common node

this dissertation, a **common node** is defined as a node incident to several subsystems in decomposed systems or a voltage measurement node.

Corollary 1:

Suppose that a common node c is connecting k subsystems S_i (i=1, 2, …, k). If all the currents incident to the common node c computed by the measured voltages and the nominal parameter values satisfy the KCL equations, i.e.,

$$\sum_{i=1}^{k} I_c^i = 0 \quad \forall t \tag{3.1}$$

$$I_c^i = h_c^{M_i}\left(v^{M_i}(t),\ f_i^0\right) \tag{3.2}$$

where I_c^i is the current incident to node c from subsystems S_i, M_i is the measurement set consisting of measurement nodes, v^{M_i} are the measured nodal voltages in subsystem S_i, f_i^0 are the nominal component values of subsystem S_i, then all subsystems S_i (i=1, 2, …, k) are fault-free.

Such a common node is called a **fault-free node**. If equation (3.1) is not satisfied, then at least one subsystem S_i is faulty. In this corollary, all decomposition nodes are measurement nodes.

Suppose now that one decomposition node x in subsystem S_i is inaccessible, i.e., the node x is still the decomposition node but its nodal voltage V_x is unknown. Thus, the decomposed subsystem topology remains unchanged, while the measurement set of S_i is

changed by removing node x. I_c^i in (3.2) can still be computed by changing the measurement set as above. The Corollary 1 is still valid to locate the fault-free subsystems.

Corollary 2:

Suppose a subsystem S_i has two fault-free nodes y and z and one of the voltages V_x in this subsystem is unknown. If the currents incident to these common nodes satisfy the KCL equations, i.e.,

$$\sum_{i=1}^{k_c} I_c^i = 0 \quad \forall t \quad c \in (y, z) \tag{3.3}$$

$$I_c^i = h_c^{M_i+X}\left(v^{M_i+X}(t),\ f_i^0\right) \tag{3.4}$$

where k_c is the number of subsystems incident to common node c, then all subsystems incident to nodes y and z are fault- free.

Here, the measurement set M_i is appended by node x. Since there is only one unknown variable V_x in (3.4), V_x can be determined uniquely because it is known that such solution exists in system-under-test. As a generalization of Corollary 2 the following lemma can be formulated.

Lemma 5:

Consider a subset of fault-free nodes in subsystem S_i with p inaccessible decomposition nodes. All p nodes are appended to the measurement set, thus leading to p

unknown variables V_{x1}, V_{x2}, …, V_{xp}. If there are m fault-free nodes and $m \geq p$, then by using m KCL equations

$$\sum_{i=1}^{k_x} I_x^i = 0 \quad x = 1, 2, \ldots, m \quad \forall t \tag{3.5}$$

$$I_x^i = h_x^{M_i + P}\left(v^{M_i + P}(t),\ f_i^0\right) \tag{3.6}$$

where k_x is the number of subsystems incident to node x, all the voltages V_{x1}, V_{x2}, …, V_{xp} can be determined and all the subsystems incident to fault-free nodes can be verified as fault-free.

Using Corollaries 1 and 2 and Lemma 5, fault-free subsystems can be sequentially verified and internal voltages determined. The system in Fig. 3.2 is used to illustrate the process.

Example 3.1

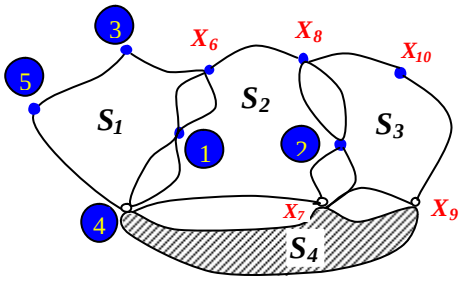

Figure 3.2 Decomposed system for example 3.1

The system shown in Fig. 3.2 is decomposed into 4 subsystems S_1, S_2, S_3, and S_4. Assume that S_4 (illustrated by the hashed area) is the only faulty subsystem. Thus, nodes {*1, 2, 3, 5,* x_6, x_8, x_{10}} are fault-free nodes. Nodes {*1, 2, 3, 4, 5*} are accessible nodes whose node indexes are circled in Fig. 3.2 and nodes $\{x_6, x_7, x_8, x_9, x_{10}\}$ are inaccessible. Apply (3.3) to nodes *3* and *5* to compute the currents I^{S1}:

$$I_{node\,3}^{S1} = h_{node\,3}^{M_{S1}+X1}\left(v^{M_{S1}+X1}(t),\ f_{S1}^{0}\right) \tag{3.7}$$

$$I_{node\,5}^{S1} = h_{node\,5}^{M_{S1}+X1}\left(v^{M_{S1}+X1}(t),\ f_{S1}^{0}\right) \tag{3.8}$$

where the measurement set is M_{s1} =[*node1, node3, node4, node5*]. Currents computed from (3.7) and (3.8) should be either zero or equal to external current excitations at these nodes. Then S_1 is concluded as fault-free by Corollary 2 and internal voltage V_{x6} is calculated.

Subsequently by applying Lemma 5 to fault-free nodes in subsystems S_2 and S_3, {*nodes 1, 2,* x_6, x_8, x_{10}} with inaccessible decomposition nodes x_7, x_8, x_9, and x_{10}, 5 equations are obtained with 4 unknown voltages. The unknown voltages V_{x7}, V_{x8}, V_{x9}, and V_{x10} can be determined and *S2* and *S3* can be verified as fault-free.

The results obtained by using Lemma 5 is based on assumption that the fault-free nodes are known, since only KCL equations in these nodes can be used to formulate the verification equations. Instead of this ad-hoc approach in Example 3.1, subsystem verification can proceed efficiently using newly developed technique described in next section for finding ambiguity groups and solving ambiguous equations.

3.3. Location of Fault-Free Nodes and Verification

A method for fault-free nodes location and their verification for a linear system with N nodes, M measurement nodes and F faulty nodes is described here. Assume that $M>F$. The system of nodal equations can be formulated as follows

$$T_0 \begin{bmatrix} V_M \\ V_X \end{bmatrix} = [W_0] + [W_F] \tag{3.9}$$

where T_0 is the nominal multi-terminal matrix of the decomposed system (size equal to the number of decomposition nodes) , V_M and V_X are voltages of measurement nodes and unknown decomposition nodes respectively, W_0 is a known excitation vector, and W_F is an unknown vector of faulty sources at faulty nodes.

Since, in general, location of fault-free nodes is unknown, it is needed to determine the unknown voltages, identify fault-free nodes and verify the fault-free equations. To this end, let us first modify (3.9) as follows

$$T_1 V_M + T_2 V_X = [W_0] + [W_F] \tag{3.10}$$

$$T_0 = [T_1 \quad T_2] \tag{3.11}$$

and move the first term from the left-hand side to the right-hand side and combine it with the right-hand side vector to get

$$T_2 V_X = [\hat{W}_o] + [W_F] \tag{3.12}$$

where

$$[\hat{W}_o] = [W_0] - T_1 V_M \tag{3.13}$$

is a known vector. Let us formulate the ambiguity group matrix

$$B = \begin{bmatrix} T_2 & \hat{W}_0 \end{bmatrix} \tag{3.14}$$

This matrix has N rows and $N-M+1$ columns.

Since the entries in vector W_F corresponding to faulty nodes are nonzero while the entries corresponding to fault-free nodes are zeroes, $N-F$ equations can be obtained from (3.12) with $N-M$ unknowns if the exact location of the faulty nodes is known. Hence, the unique solution to all V_X can be determined. To avoid a combinatorial search for faulty nodes, the ambiguity groups locating technique in Section 2.3.2 can also be utilized here to efficiently locate all fault-free nodes. It is based on QR factorization to find a numerically stable solution of over determined system. The primary idea is to find dependent relationship among the rows of matrix B, that is, to identify the ambiguity groups in (3.12) with the maximum size. The QR factorization and swapping is applied together with corresponding theoretical results described in Section 2.3.2. A new lemma is developed below to locate the maximum number fault-free nodes.

Lemma 6:

If $M>F$ and matrix B has full column rank ambiguity group, then the row indices of the sub-matrix which form this ambiguity group are fault-free nodes, and all the subsystems incident to these nodes are fault free.

Example 3.2

Example 3.2 is provided to illustrate the location of fault-free nodes. The system has 6+1 nodes with one of nodes being reference. The measurements are taken on nodes

{*1, 3, 6*} whose node indexes are circled in Figure 3.3 and the fault-free nodes are nodes {*1, 4, 5, 6*} which are points filled in black. The parameters are as below:

$$T_0 = \begin{bmatrix} 1 & 0 & 5 & -2 & 0 & 6 \\ 0 & 2 & 0 & 7 & 9 & 3 \\ 5 & 0 & 3 & -1 & 0 & 0 \\ -2 & 7 & -1 & 4 & 7 & 8 \\ 0 & 9 & 0 & 7 & 5 & 7 \\ 6 & 3 & 0 & 8 & 7 & 6 \end{bmatrix} \qquad W_0 = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad J_F = \begin{bmatrix} 0 \\ -2 \\ -3 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad V_M = \begin{bmatrix} V_1 \\ V_3 \\ V_6 \end{bmatrix} = \begin{bmatrix} -0.2455 \\ -0.4437 \\ 0.7245 \end{bmatrix}$$

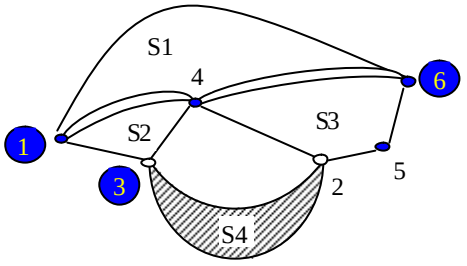

Figure 3.3 Fault-free nodes location for example 3.2

By (3.14), *6x4* matrix *B* is obtained for analysis. Applying ambiguity group locating techniques in Section 2.3.2, a *4x2* linear combination matrix *C* is obtained after QR factorization and column swapping as follows

$$C = \begin{bmatrix} -1.7500 & -1.0000 \\ -4.8869 & -4.0714 \\ 2.5357 & 1.7143 \\ 0.6667 & 0.0000 \end{bmatrix}$$

with its basis including nodes {*5, 1, 4, 3*} and co-basis nodes {*2, 6*}. The unique zero entry in *C* indicates that the ambiguity group {*5, 1, 4, 6*} is located. According to Lemma 6, this group contains fault-free nodes.

The above method to locate fault-free nodes is based on linear nodal analysis, thus is only applicable to linear system. For nonlinear network, Lemma 6 can be used to implement the location of fault-free nodes with incident current I_c^i computed by (3.2). Note that in a nonlinear system only measurement nodes should partition the nonlinear systems.

After location of fault-free nodes and faulty subsystems, computation efforts required by faulty parameter location are limited. Since there is no strict requirement for computer memory and testing time in today's medium or small scale analog test, the choice for faulty parameter location techniques inside faulty subsystem is versatile such as the techniques provided in part V of [43] or the techniques provided by other references for linear analog networks [21, 39] and for nonlinear analog networks [13].

For the linear network, equation (30) in [43] can be utilized to compute external currents. For the network with faulty nonlinear parameters, fault model of nonlinear components can be utilized to locate faulty nonlinear parameters. For the network with faulty linear parameters and fault-free nonlinear parameters, utilize nonlinear system solver such as Pspice to locate the faults.

3.4. Example Circuit

To illustrate the efficiency of the developed approach and to compare the developed approach and the method in [43], Example 5 in [43] is selected. Figure 3.4 is the first stage of analog filter benchmark circuit. The equivalent circuit for operational amplifier is outlined in Figure 2.6. The nominal circuit component values are the same as

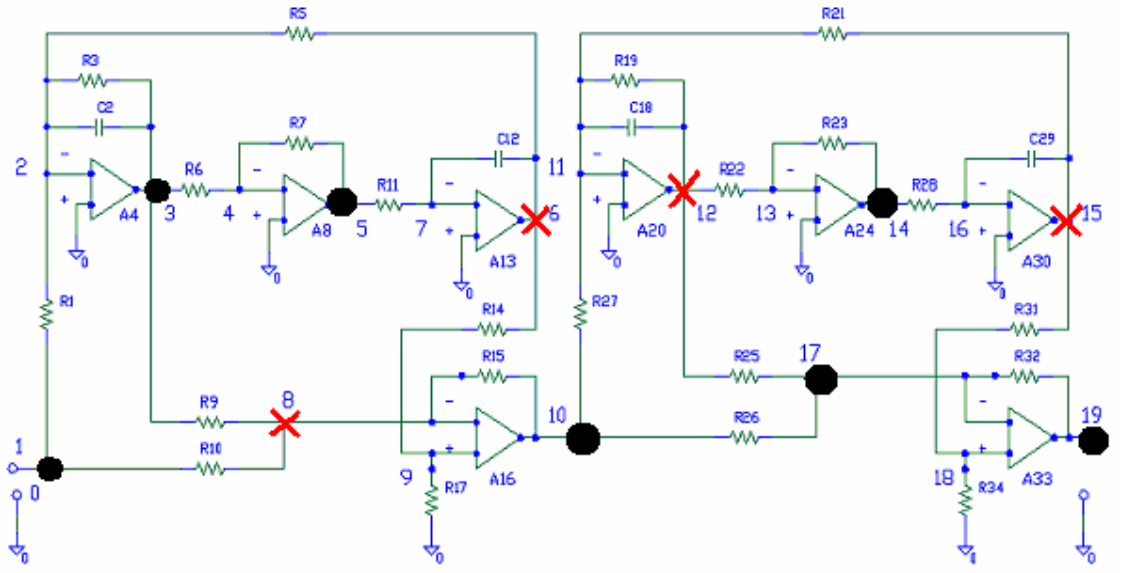

Figure 3.4 Active low-pass filter

that illustrated in Figure 9 of [43]: (all resistors in $k\Omega$ and capacitors in mF): $R_1=0.182$, $C_2=0.01$, $R_3=1.57$, $R_5=2.64$, $R_6=10.0$, $R_7=10.0$, $R_9=100.0$, $R_{10}=11.1$, $R_{11}=2.64$, $C_{12}=0.01$, $R_{14}=5.41$, $R_{15}=1.0$, $R_{17}=1.0$, $C_{18}=0.01$, $R_{19}=4.84$, $R_{21}=2.32$, $R_{22}=10.0$, $R_{23}=10.0$, $R_{25}=500.0$, $R_{26}=111.1$, $R_{27}=1.14$, $R_{28}=2.32$, $C_{29}=0.01$, $R_{31}=72.4$, $R_{32}=10.0$, $R_{34}=10.0$. The decomposed subsystems and the corresponding indexes of subsystems are also the same as those in Figure 9 of [43]. For convenience, the decomposed structure is shown in Fig. 3.5 here.

The faulty components are $R_{15}=0.2kW$, $R_{17}=2.0kW$, $R_{27}=11.14$ kW, and $C_{18}=0.1mF$ which lead to faulty nodes {*8, 9, 10, 11, 12*}. The measurement set contains nodes {*1, 3, 5, 10, 14, 17, 19, 37*} which are filled black points. The unknown nodal

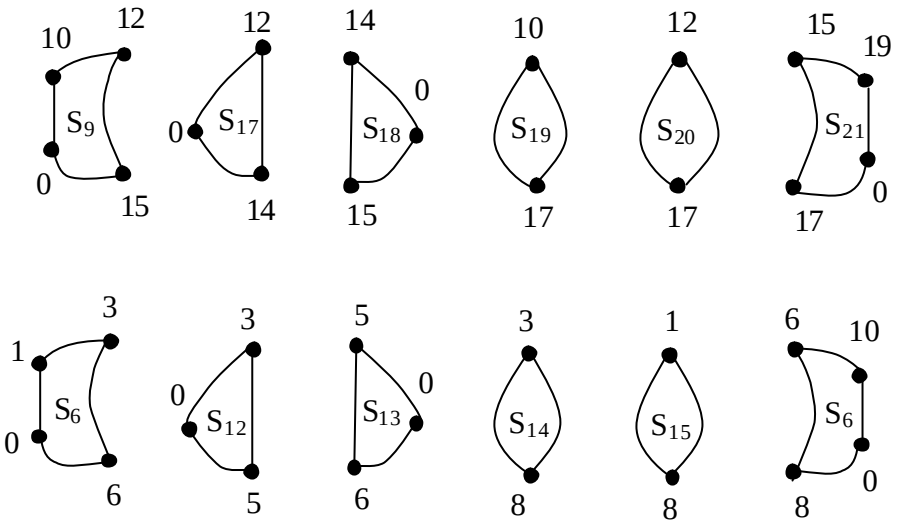

Figure 3.5 Decomposed subsystems

voltages at nodes {*6, 8, 12, 15*} which are red cross are to be solved by the developed approach and fault-free nodes determined. Hence, *N=37, M=8, F=5* and *M>F*. The sinusoidal current source to node *1* is $j(t) = 0.01\cos(2000\,t)A$. Notice that with these limited measurements, the method presented in [43] would not apply since there is no single fault-free node with all incident subsystem voltages measured.

The first step is to locate the fault-free nodes by the techniques in Section 3.3. The *37x31* matrix *B* is constructed by circuit nominal values and measurement vector V_M. After QR factorization and swapping operations, a *31x6* linear combination matrix *C* is obtained. The ambiguity group located is {*1—7, 13—37*} which matches the fault-free nodes in real case. The second step is to decompose the system into subsystems by measurement nodes plus nodes {*6, 8, 12, 15*}.

Applying Lemma 5 to fault-free nodes {*1, 3, 5*}, 3 equations with 2 variables V_6 and V_8 can be obtained as follows

$$
\begin{aligned}
0 &= I_1^{S6} + I_1^{S15} + J \\
&= \left(-8.519 \times e^{-3} + 7.236 \times e^{-4}\ i + V_6 \times (-3.197 \times e^{-4} + 9.821 \times e^{-7}\ i)\right) \\
&\quad + \left(-9.848 \times e^{-3} + 7.867 \times e^{-7}\ i + V_8 \times (-9.009 \times e^{-5})\right) + (1.000 \times e^{-2}) \\
0 &= I_3^{S6} + I_3^{S12} + I_3^{S14} \\
&= \left(-1.415 \times e^{2} + 1.228 \times e^{1}\ i + V_6 \times (-5.818 + 1.787 \times e^{-2}\ i)\right) \\
&\quad + \left(-1.049 \times e^{-5} - 1.284 \times e^{-4}\ i\right) + \left(6.462 \times e^{-5} - 1.834 \times e^{-5}\ i\right) \\
0 &= I_5^{S12} + I_5^{S13} \\
&= \left(-4.072 \times e^{-5} - 4.865 \times e^{-4}\ i\right) \\
&\quad + \left(-2.551 \times e^{-5} + 3.446 \times e^{-6}\ i + V_6 \times (-1.053 \times e^{-6} - 1.994 \times e^{-5}\ i)\right)
\end{aligned}
$$

After solving and verifying, the solution vector is

$$[V_6\ V_8] = [-24.329 + 2.0362\,i \qquad -6.5672 + 0.54964\,i]$$

Similarly, by applying Lemma 5 to fault-free nodes {*14, 17, 19*}, 3 equations with 2 variables V_{12} and V_{15} can be obtained and the solution vector is

$$[V_{12}\ V_{15}] = [\ 6.912e-3 + 6.629 \times e^{-2} \qquad 1.429 - 1.522 \times e^{-1}\ i]$$

According to Lemma 5, subsystems {S_9, S_{16}} are declared as faulty. To locate and verify the faulty parameters, techniques in Section 2.3.2 is utilized. The faulty parameters are declared as {R_{15}, R_{17}, R_{27}, C_{18}} which are the exact answer.

3.5. Conclusion

To address the increased complexity and reduced accessibility problems in large-scale analog testing that dominate the market of mixed-signal systems or SoC products in

recent years, fault location by decomposition technique is generalized in this chapter. The system topology and the nominal parameter values are available before testing. The decomposition of the whole system into subsystems is implemented and ambiguity group finding technique is used to locate fault-free decomposition nodes. While in the traditional decomposition techniques only the accessible nodes can be decomposition nodes, in this chapter some inaccessible nodes can also be used as the decomposition nodes. A new approach developed in this chapter calculates inaccessible nodes nodal voltages under faulty condition. The benefits resulting from this work include reduction of test requirements for the number of accessible nodes and increase in the flexibility of decomposition. By checking the consistency of KCL equations for the decomposition nodes, faulty subsystems and subsequently faulty parameters can be located. Testing conditions are independent of the system and excitation types, thus this approach is applicable to both linear and nonlinear systems, and to both time domain and frequency domain. The developed technique is particularly effective for large-scale analog systems with limited accessibility. The same example circuit as that in classic decomposition research is utilized to demonstrate the efficiency of the developed technique with positive results.

CHAPTER 4 LOCATING CATASTROPHIC FAULTS

4.1. Stuck Fault Model and Catastrophic Fault Location

Lack of effective fault model is another problem for analog test and fault diagnosis. Simultaneously, digital test is much more developed than analog test. Conceivably, some analog test researchers and test engineers tried to apply some successful digital fault models to the area of analog test. This is a promising strategy because Design-for-Testability (DFT) and Built-in-Self-Test (BIST) in analog and mixed signal test are two obvious and successful examples that utilize the working paradigms used in digital test. As the most widely used fault model in digital test, stuck-at-1/0 model combined with output logic level monitoring can also find its counterpart in analog test. In digital stuck-at 1/0 model, it is assumed that all failure mechanisms manifest themselves as a single node stuck at logic 0 or 1. Based on this model, many digital test algorithms and techniques were developed [50].

There are two kinds of faults in the test area: parametric (soft fault) and catastrophic (hard) faults. When circuit parameter is deviated from its nominal value more than its allowed tolerance, it is called a parametric fault. The techniques discussed in former chapters are very effective to test and diagnose those parametric faults. Catastrophic faults such as open circuit and short circuit are serious faults, and most of faults occurring in reality are catastrophic faults. Fig. 4.1 illustrates a broken signal line in CMOS circuit manufacturing. In Fig. 4.2, a signal line is open, connected with another signal line (bridging fault), or shorted to the ground.

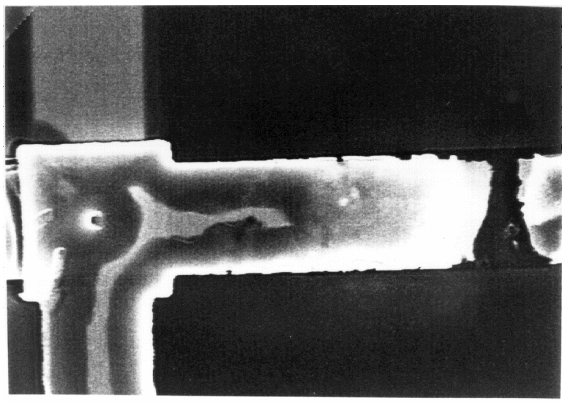

Figure 4.1 Broken signal line in analog manufacturing

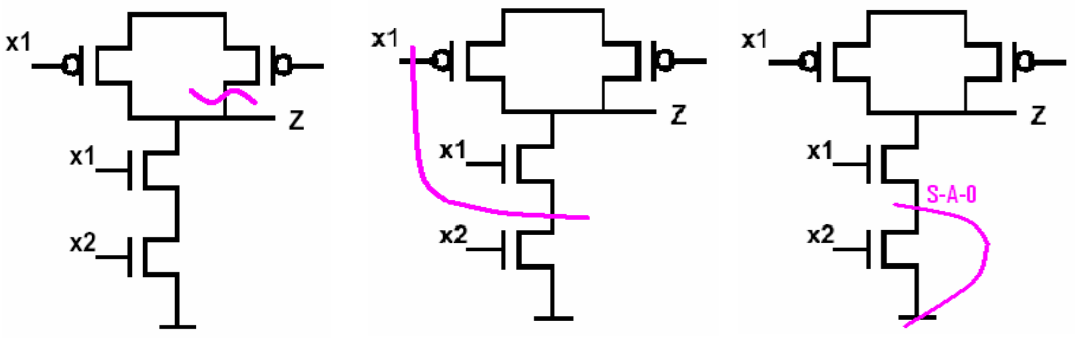

Figure 4.2 Open fault, bridging fault, and short-to-ground fault

Since analog manufacturing and digital manufacturing process are almost the same, stuck-at 1/0, bridging, and stuck-open faults also happen in analog manufacturing process, especially with today's increased complexity and increased die size of analog chips originated from different short, bridging or open failure mechanisms. The models of stuck-at, bridging and stuck-open faults have been reported in [4, 25-28, 51] and their applications are from analog fault simulation [4, 52], test generation [4, 52], to fault detection [53]. To test and diagnose these faults, the primary tactics of these fault-based

approaches are to utilize a dictionary approach through a comprehensive simulation on the circuit with inserted fault model before the test. Fault detection and location is determined by the comparison between measured signature and the signature precompiled and stored in the fault dictionary. Hence it requires many simulations and extensive fault dictionary.

In this chapter, an ideal switch is utilized to model those catastrophic faults and a new approach is developed to locate multiple stuck-at 1/0, bridging and stuck-open faults by verification approach without repetitive simulation needed for fault dictionary [54]. An ideal open switch is inserted between the potential faulty nodes under fault-free condition. The switch is closed to connect two different circuit nodes together to model bridging fault (Fig. 4.3). A switch is inserted between the potential faulty node and the potential fault source – voltage source or ground. It is closed under faulty state to model stuck-at-1/0 fault (Fig. 4.4). To model a stuck-open fault, a switch is inserted in series with a line or a component. It is open when stuck-open fault occurs (Fig. 4.5). Simultaneously, such a serial switch together with an unknown-value admittance component can model the parametric faults.

In Section 4.2, constitutive equations of ideal switches derived from the KCL are combined with the other constitutive equations of circuit parameters to construct modified nodal equations for the newly resulting circuit. Note that the ideal switches do not exist physically in the circuits. The ambiguity group locating technique in Section 2.3.2 for multiple analog fault diagnosis is utilized to detect and locate all these faults exactly based on the limited measurements of circuit responses in Section 4.3. There is no

need for repetitive simulation comparing with other catastrophic faults location techniques such as fault dictionary approach. The effect of locating stuck-at, bridging and stuck-open faults is modeled with full precision of resulting test conditions. In Section 4.4, an analog IC - μA741 is given as an example. Conclusions are drawn in Section 4.5.

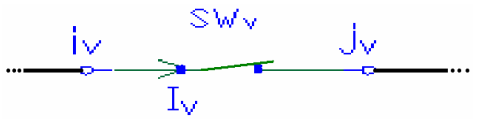

Figure 4.3 Bridging fault

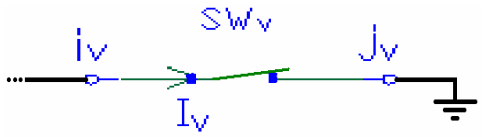

Figure 4.4 Stuck-at-0 fault

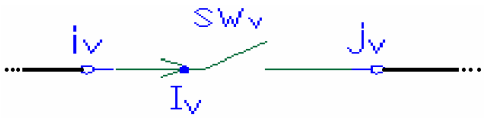

Figure 4.5 Stuck-open fault

4.2. Application of Stuck-at, Bridging and Stuck-Open Model

Based on the same assumptions as those in Chapter 2, applying KCL to each node of the CUT and all circuit parameters that do not have an admittance description, the

same modified nodal equations as the one in Chapter 2 (Equation 2.1) is obtained. It is re-written as follows for convenience:

$$T_g X_g = W_g \tag{4.1}$$

Assume that research interests are only focusing on s potentially stuck faults in the CUT: ss of s are stuck-at and bridging faults and so of s are stuck-open faults($s=ss+so$). The ideal open switch SW_v *(v=1, 2, … ss)* is inserted between each pair of nodes i_v and j_v which has a potential for a bridging fault. Nodes i_v or j_v is connected to voltage source for stuck-at-1 fault, or ground for stuck-at-0 fault. Current I_v flows from node i_v to node j_v [Fig. 4.6]. For stuck-open fault, a shorted switch SW_v ($v=1, 2, \ldots, so$) is between i_v and a newly created node j_v.

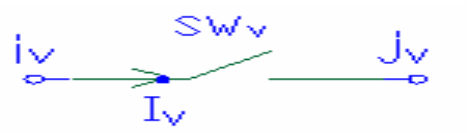

Figure 4.6 A model of ideal open switch

According to KCL, the constitutive equation to describe the ideal switch SW_v is as follows:

$$F(V_{i_v} - V_{j_v}) + (F-1)I_v = 0 \tag{4.2}$$

where variable F is 0 for the open switch and 1 for the closed switch [35]. Totally, s such equations are obtained.

Simultaneously, current I_v is added to KCL equation at node i_v while I_v is subtracted from KCL equation at the node j_v. Therefore, the coefficient matrix of the modified nodal equations is augmented by one ideal switch SW_v [Fig. 4.7].

$$\begin{array}{c} \\ i_n \\ j_n \\ \\ g+1 \end{array} \begin{array}{c} \begin{array}{cccc} i_n & j_n & & g+1 \end{array} \\ \begin{bmatrix} X & X & \vdots & 1 \\ X & X & \vdots & -1 \\ \cdots & \cdots & \cdots & \cdots \\ F & -F & \vdots & F-1 \end{bmatrix} \end{array}$$

Figure 4.7 Modified coefficient matrix with an inserted switch

The resulted modified nodal equation with all *s* switches is as follows:

$$\begin{bmatrix} T_g & e_{i_1}-e_{j_1} & e_{i_2}-e_{j_2} & \cdots & e_{i_s}-e_{j_s} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ F_1\left(e_{i_1}-e_{j_1}\right)^T & F_1-1 & & & \\ F_2\left(e_{i_2}-e_{j_2}\right)^T & & F_2-1 & & \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ F_s\left(e_{i_s}-e_{j_s}\right)^T & & & & F_s-1 \end{bmatrix} \begin{bmatrix} X_g \\ I_1 \\ I_2 \\ \cdots \\ I_s \end{bmatrix} = \begin{bmatrix} W_g \\ 0_{sx1} \end{bmatrix} \qquad (4.3)$$

where I_{sxs} is a sxs unit matrix, and 0_{sx1} is a $sx1$ zero vector.

Let us define an gxs matrix A which is to describe the locations of ideal switches in the circuit:

$$A = \left| e_{i_1}-e_{j_1} \;\; e_{i_2}-e_{j_2} \ldots e_{i_s}-e_{j_s} \right| \qquad (4.4)$$

And let F be a diagonal sxs matrix of switch values

$$F=\begin{bmatrix} F_1 & & & \\ & F_2 & & \\ & & \cdots & \\ & & & F_s \end{bmatrix}$$

Hence, the coefficient matrix in (4.3) has the following form

$$\begin{bmatrix} T_g & A \\ FA^T & (F-1)I_{sxs} \end{bmatrix}$$

For fault-free circuit, all switches in stuck-at and bridging models are open, i.e., *F=0*. For faulty circuit, only switches corresponding to stuck-at and bridging faults are closed, i.e., $F_k=1$, while the remaining switches are still open. This observation is reversed for the stuck-open models.

For simplicity, all switches in stuck-at and bridging models are separated with all switches in stuck-open models in modified nodal equation (4.3), which can be implemented by matrix permutation. Hence, matrix *A* is separated as

$$A = [A_{ss} \;\; A_{so}] \tag{4.5}$$

Applying (4.3) to fault-free circuit, we will obtain

$$T_0 X_0 = W_0 \tag{4.6}$$

where X_0 is an *(g+s)x1* solution vector, W_0 is an *(g+s)x1* excitation vector, and *(g+s)x(g+s)* coefficient matrix

$$T_0 = \begin{bmatrix} T_{g0} & A_{ss} & A_{so} \\ 0_{ssxg} & -I_{ssxss} & 0_{ssxso} \\ A_{so}^T & 0_{soxss} & 0_{soxso} \end{bmatrix}$$

Suppose that only *f* of *s* stuck faults really occurred in the faulty circuit. Among *f* faults, there are *fs* of *ss* stuck-at and bridging faults and *fo* of *so* stuck-open faults (*f=fs+fo*). Therefore, only *fs* of *ss* switches in stuck-at and bridging models are closed while the remaining *ss-fs* switches are still open. Similarly, *fo* of *so* switches in stuck-open models are open, while the remaining *so-fo* switches are closed. Assume that excitations for faulty circuit are the same as those of fault-free circuit, and all *f* switches are permuted for simplicity such that all *fs* and *fo* switches are ordered first among *ss* and *so* switches, respectively. The modified nodal equation for faulty circuit is:

$$TX = (T_0 + \Delta T)(X_0 + \Delta X) = W_0 \tag{4.7}$$

$$T = T_0 + \Delta T \tag{4.8}$$

$$X = X_0 + \Delta X \tag{4.9}$$

where

$$T = \begin{bmatrix} T_{g0} & A_{gxfs} & A_{gx(ss-fs)} & A_{gxfo} & A_{gx(so-fo)} \\ A_{fs}^T & 0_{(ss-fs)xfs} & 0_{(ss-fs)x(ss-fs)} & 0_{(ss-fs)xfo} & 0_{(ss-fs)x(so-fo)} \\ 0_{(ss-fs)xg} & 0_{(ss-fs)xfs} & -I_{(ss-fs)x(ss-fs)} & & \\ 0_{foxg} & & & -I_{foxfo} & \\ [A_{so} \mid A_{fo}]^T & & & & 0_{(so-fo)x(so-fo)} \end{bmatrix} \tag{4.10}$$

$$\begin{aligned} A_f &= \lfloor A_{fs} \; A_{fo} \rfloor \\ &= [e_{i_1} - e_{j_1}, e_{i_2} - e_{j_2}, \ldots, e_{i_{fs}} - e_{j_{fs}}, e_{i_{fs+1}} - e_{j_{fs+1}}, \ldots e_{i_f} - e_{j_f}] \end{aligned} \tag{4.11a}$$

$$A = \lfloor A_{gxfs} \; A_{gx(ss-fs)} \quad A_{gxfo} \quad A_{gx(so-fo)} \rfloor \tag{4.11b}$$

$$\Delta T = \begin{bmatrix} 0_{gxg} & 0_{lxfs} & 0_{lx(ss-fs)} & 0_{lxfo} & 0_{lx(so-fo)} \\ A_{fs}^T & I_{fsxfs} & & & \\ 0_{(ss-fs)xg} & & 0_{(ss-fs)x(ss-fs)} & & \\ -A_{fo}^T & & & -I_{foxfo} & \\ 0_{(so-fo)xg} & & & & 0_{(so-fo)x(so-fo)} \end{bmatrix} \quad (4.12)$$

In (4.10), $[A_{so} \mid A_{fo}]$ denotes removing sub-matrix A_{fo} from the matrix A_{so}. Define two $(g+s)xf$ matrices P_f and Q_f as follows:

$$P_f = \begin{bmatrix} 0_{gxf} \\ I_{fsxfs} \mid 0_{fsxfo} \\ 0_{(ss-fs)xf} \\ 0_{foxfs} \mid I_{foxfo} \\ 0_{(so-fo)xfs} \end{bmatrix} \quad (4.13)$$

$$Q_f = \begin{bmatrix} A_{fs} \mid -A_{fo} \\ I_{fsxfs} \mid 0_{fsxfo} \\ 0_{(ss-fs)xf} \\ 0_{foxfs} \mid -I_{foxfo} \\ 0_{(so-fo)xf} \end{bmatrix} \quad (4.14)$$

then ΔT is the matrix product of P_f and Q_f^T:

$$\Delta T = P_f Q_f^T \quad (4.15)$$

and (4.7) can be re-written as

$$(T_0 + P_f Q_f^T)(X_0 + \Delta X) = W_0 \quad (4.16)$$

After substituting (4.6) into (4.16), ΔX can be solved by

$$\Delta X = - T_0^{-1} P_f \; Q_f^T X \tag{4.17}$$

Denote an $(l+s)x(l+s)$ matrix S_0 as follows

$$S_0 = [s_1 \; s_2 \; \ldots \; s_{g+s}] = -T_0^{-1} \tag{4.18}$$

and rewrite vector X in a scalar form:

$$X = [x_1 \; x_2 \; \ldots \; x_g \; I_1 \; I_2 \ldots I_s]^T \tag{4.19}$$

where $s_v \; (v = 1, 2, \ldots, g + s)$ is an $(g+s)xg$ vector while $x_v \; (v = 1, 2, \ldots, g)$ and $I_v \; (v = 1, 2, \ldots, s)$ are numbers.

Denote the matrix product of S_0 and P_f as S_F, and product of Q_f^T and X as l_F:

$$\begin{aligned} S_F &= S_0 P_f = [s_{g+1} s_{g+2} \ldots s_{g+fs} \; s_{g+ss+1} s_{g+ss+2} \ldots \; s_{g+ss+fo}] \\ l_F &= Q_f^T X = [x_{i_1} - x_{j_1} + I_1, \; x_{i_2} - x_{j_2} + I_2, \; \ldots, \\ &\qquad x_{i_{fs}} - x_{j_{fs}} + I_{fs}, - x_{i_{fs+1}} + x_{j_{fs+1}} - I_{ss+1}, \\ &\qquad - x_{i_{fs+2}} + x_{j_{fs+2}} - I_{ss+2}, \ldots, - x_{i_f} + x_{j_f} - I_s]^T \end{aligned} \tag{4.20}$$

where the **faulty set** F represents the set of all the stuck faults and S_F is an $(g+s)xf$ matrix while l_F is an $fx1$ vector.

Now (17) can be re-written as

$$\Delta X = S_F \; l_F \tag{4.21}$$

The remaining work is to analyze this equation by limited measurements of circuit responses. Assume that the first m elements of ΔX can be measured and $f + 1 < m < s$, following equation can be obtained

$$\begin{bmatrix} \Delta X^{M} \\ \Delta X^{L+S-M} \end{bmatrix} = \begin{bmatrix} S_{MF} \\ S_{L+S-M,F} \end{bmatrix} l_F \tag{4.22}$$

Thus, the following **test equation** is obtained by only considering the first part of the above equation:

$$S_{MF}\ l_F = \Delta X^{M} \tag{4.23}$$

Here S_{MF} is an *mxf* matrix whose columns correspond to stuck faults in the CUT. Similarly S_{MS} is an *mxs* matrix whose columns correspond to all of the potential stuck faults in the CUT, where *S* indicates the set of all potential faults, i.e., all ideal switches. The test equation (4.23) plays an important role in relating the limited circuit output measurements with the stuck faults in a linear way.

4.3. Stuck Fault Location

To locate stuck faults in the CUT, let us analyze the test equation. The right-hand side of (4.23) is a known vector and the left-hand side is the product of an unknown coefficient matrix S_{MF} and an unknown solution vector l_F. Note that matrix S_{MF} is the set of selected columns of the known matrix S_{MS}. The columns of S_{MF} correspond to the locations of switches, i.e., stuck faults while the columns of S_{MS} correspond to the locations of all inserted switches. And matrix S_{MS} has more columns than rows since $m < s$ by restriction in Section 4.2. The idea in this work to identify the faults is to identify the minimum size ambiguity group in test equation by finding the minimum number of independent columns in matrix S_{MS} that satisfy test equation. The numerically efficient

ambiguity group locating technique in Section 2.3.2 to multiple analog fault location is utilized here to identify stuck faults.

An important observation is that the process derived in Section 4.2 only considers stuck-at, bridging and stuck-open faults ignoring circuit parametric deviations for simplicity. Hence, parameter verification is omitted and only fault detection and location in fault diagnosis are discussed here. However, the developed approach can be applied to the mixed fault condition – multiple stuck-at, bridging, stuck-open faults and multiple parametric faults. Test equation (4.23) still holds while only the structural matrices A, A_f must be expanded to include the parametric faults. Consequently, parameter verification is required after the fault location.

4.4. Example Circuit

The classical Fairchild *mA741* operational amplifier is selected to demonstrate the developed approach. A simplified schematic of *mA741* is shown in Fig. 4.8 [35]. The negative feedback configuration is the circuit under test [Fig. 4.9] with a small signal voltage input $V_{in}(t) = 0.01 \sin 120\,pt$. The small signal model of bipolar junction transistors (BJT) in Fig. 4.10 is applied to all 18 BJTs for simplicity. There are 21 nodes, 48 resistors, and 18 voltage-controlled-current sources in the CUT. The nominal values of circuit parameters are indicated in figures. Note that the external potentiometer R_{EXT} in Fig. 4.8 is equally divided into two resistors with a value of $5kW$.

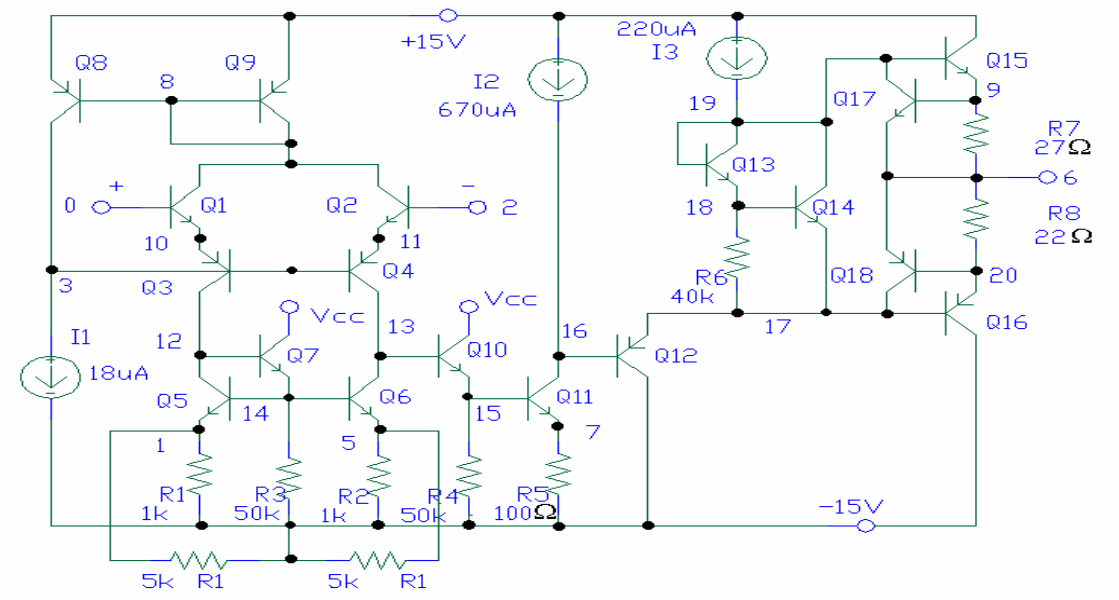

Figure 4.8 A overall schematic of the Fairchild µA741 operational amplifier

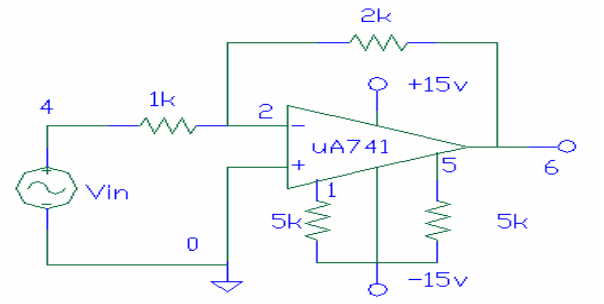

Figure 4.9 Negative feedback configuration of µA741

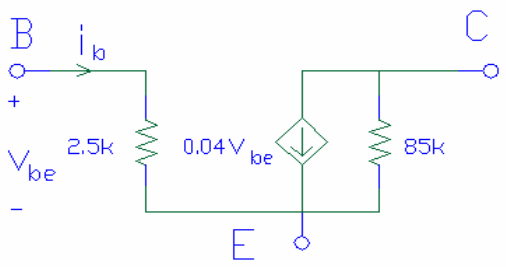

Figure 4.10 The small signal model of BJT

For simplicity, only 5 suspicious stuck-at-0 faults are considered that are located between node pairs {*9, 0*}, {*12, 0*}, {*13, 0*}, {*15, 0*}, {*17, 0*}. Thus 5 open ideal switches are inserted between these nodes pairs. The first two ideal switches are supposed to be closed in the faulty circuit. Nodal voltages are measured at nodes {*3, 6, 14, 16*}. Hence, *n=20, f=2, s=5, m=4* and *f+1<m<s*. The measured nodal voltage deviations are

$$\Delta X^{M} = \begin{bmatrix} -4.4781 \times e^{-4} \\ -2.8747 \times e^{-3} \\ -7.8085 \times e^{-3} \\ -4.3321 \times e^{-2} \end{bmatrix}$$

which obviously is not a zero vector indicating that faults are detected.

Applying ambiguity group locating technique to test equation, a *3x2* matrix *C* is obtained after Gaussian elimination and QR factorization with column permutation {*3, 2, 4, 1, 5*}:

$$C = \begin{bmatrix} 1.6679 \times e^{-15} & 5.1167 \times e^{-4} \\ 4.3052 \times e^{-3} & 1.1034 \times e^{-2} \\ -1.6813 \times e^{-13} & -5.1821 \times e^{-2} \end{bmatrix}$$

Thus the basis of ambiguity group is {*3, 2, 4*} which correspond to the 3rd, 2nd, and 4th switches respectively. The co-basis is {*1, 5*} corresponding to the 1st and 5th switches.

By analyzing matrix C, there is only one suspicious ambiguity group {*1, 2*}. According to the algorithm in Fig. 2.3, this is the minimum size ambiguity group. The conclusion is drawn that switches {*1, 2*} are closed, i.e., there are two stuck-at-0 faults on nodes pairs {*9, 0*} and {*12, 0*}, which are the exact solutions for this CUT.

4.5. Conclusions

Because analog and mixed signal test and fault diagnosis are less advanced than digital test, conceivably, digital test techniques greatly influence the analog test. As a widely used paradigm in digital test, stuck-at model together with the output monitoring have been applied to analog area to model open, bridging or short failure mechanisms. These fault models are increasingly important for today's SoC solutions with increased complexity and increased die size of analog and mixed signal designs. In this chapter, such models are utilized to locate faults by verification approach rather than by dictionary approach typically used in such case. With the known circuit topology, ideal switches are inserted to connect the suspicious circuit nodes. Under normal conditions, all ideal switches are open (closed) while some of them are closed (open) under faulty conditions. The circuit topology is modified by inserted switches and new modified nodal equation is established based on KCL equations. A newly developed approach to multiple fault diagnosis is applied to identify the faults.

Avoiding the combinatorial search of suspicious stuck-at and stuck-open faults reduces computation cost of multiple fault location. The developed approach can also be applied to the mixed faults condition – multiple stuck-at, bridging, and stuck-open faults together with multiple parametric faults. Finally, a commercial analog IC is provided as an example to demonstrate the developed approach.

CHAPTER 5 CONCLUSIONS

5.1. Summary of the Research Results

With fast development in mixed-signal systems and System-on-Chip products, there is an urgent need to develop effective, highly automated and systematic paradigms for analog and mixed-signal test and fault diagnosis. One driving force which stems from economic considerations is to reduce test cost and time. Another one stems from the fact that in today's analog test area: analog test lags far behind digital test and the computer-aided test software is less developed than the design software. So that the ratio of analog test cost to system test cost is disproportionally higher than the ratio of analog area to the whole system. The significance of the research in this area is to keep a reasonable balance for different blocks tests within a complex system. Analog test is also beneficial to correcting design flaws, reducing time-to-market, increasing manufacturing yield, and reducing a system cost. There are several challenging problems in analog and mixed-signal test and fault diagnosis. Ambiguities such as tolerance, nonlinearity and limited measurements prevent us from accurate computation and accurate measurement. Increased complexity and reduced accessibility exist in today's highly integrated systems. There is no effective analog fault model to relate fault coverage with performance. Finally, an increased analog test cost is becoming the bottleneck for mixed-signal system development.

All analog test problems mentioned above are explored in this dissertation [Chapter 2-4]. Based on the ambiguity group locating technique, a verification technique

is developed in Chapter 2 to address the ambiguity problem for the purpose of accurate computation. Circuit topology and nominal circuit parameters are known before test. Different methodologies in excitation, measurement, mathematical tools, and network theory are utilized to establish a fault diagnosis equation to relate the limited measurements with faulty parameters in a linear way. Ambiguity group locating technique is developed to efficiently search for a minimum size ambiguity group. This group can satisfy the fault diagnosis equation and is critical for the final solution of faulty parameters. After location of a minimum ambiguity group, deviations and other parameters under faulty case can be accurately computed and verified. Simultaneously, an advanced technique to eliminate the Gaussian elimination and swapping operations in the ambiguity group locating technique is developed to reduce more computational cost. It is based on multiple excitations and multiple measurements approaches. The experiments on example circuits are positive for those verification techniques.

Verification techniques developed in Chapter 2 can accurately compute parameter deviations. They are extremely effective for analog circuit with very limited accessible nodes. Comparing with combinatorial search in traditional fault verification approaches, computation cost is greatly reduced.

To address the problems of complexity and accessibility, a large scale system is decomposed into smaller subsystems. In a typical decomposition approach, all decomposition nodes have to be accessible for voltage measurement. This restriction on accessibility is removed in Chapter 3, so that some specific inaccessible nodes can be used as decomposition nodes by computing their nodal voltages. Fault-free nodes among decomposition nodes are first located by ambiguity group finding technique. Then, faulty

subsystems and subsequently faulty parameters can be located by checking consistency of KCL equations on the decomposition nodes. New lemmas and corollaries are proposed to calculate nodal voltages of inaccessible nodes under faulty condition if the lemma/corollary conditions are satisfied.

The contribution of this work lies in the fact that test requirements for accessibility is relieved and that the decomposition flexibility is increased. The developed technique is particularly effective for large-scale analog systems with limited accessibility. It can be applied to linear and nonlinear systems in both time domain and frequency domains. The same benchmark circuit as that in traditional decomposition approach is utilized to illustrate the efficiency and improvement of the generalized decomposition over traditional decomposition.

Digital stuck-at-1/0 model is successful in modeling catastrophic faults in digital test. In Chapter 4, ideal switch is used in stuck fault model for analog catastrophic faults such as open, short and bridging. These fault mechanisms are frequently encountered in mixed-signal system and SoC market. For each faulty case, one switch is inserted. It is open or close corresponding to faulty or fault-free condition. The system equation is expanded by appending to it all switches' constitutive equations. To locate multiple analog catastrophic faults, a location approach by verification is designed eliminating repetitive simulation requirement among traditional stuck faults location techniques – for instance in a dictionary approach. The developed approach can also be applied to the mixed faults condition – multiple stuck-at, bridging, and stuck-open faults, together with multiple parametric faults. Simulation experiment on a commercial analog IC successfully locates all the stuck faults.

Significant increasing cost and time is absolutely the most critical problem in analog test. How to reduce test time and reduce one of the test cost, computational cost, is present in all the research efforts in this dissertation. The repeating pattern in all research works is to develop computer-aided techniques for fast and computationally efficient testing [55].

5.2. Recommended Future Work

In this dissertation, most analog test problems are explored. Due to the time limits, some problems are not on the research list.

Examples of ambiguities problems consist of limited measurement, tolerance and non-linearity. Verification techniques are to address the problem of limited measurements, but the problems of tolerance and non-linearity are left out. The future research to find out some solutions to these two ambiguity problems is expected.

Although the stuck fault model can represent the catastrophic faults in analog manufacturing, some researchers pointed out that the real catastrophic fault mechanism in analog circuits is much more complicated [4]. Until now, the researchers do not have a full understanding about the analog catastrophic fault mechanism. More explorations are needed in future and a new analog fault model is strongly needed.

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ABSTRACT

Liu, Dong, Ph. D August, 2003

Electrical Engineering

Analog and Mixed Signal Test and Fault Diagnosis (109 pp.)

Director of Dissertation: Dr. Janusz A. Starzyk

Analog and mixed-signal test and fault diagnosis play an essential role in circuit design, device production, and instrumentation maintenance. The driving forces for this research consist of economic factors such as time/cost consideration, and the fact that analog test and diagnosis lags far behind digital test. The benefits include correcting design flaws, reducing time-to-market, increasing manufacturing yield, and reducing the system cost. Fault diagnosis has three tasks: fault detection to find the faulty systems, fault location to identify the faulty parameters, and parameter evaluation to calculate deviations. The difficulties for analog and mixed-signal test and fault diagnosis are coming from ambiguities, increased complexity, reduced accessibility, lack of effective fault models, and increasing test cost.

In this dissertation, above problems are explored. A verification technique based on the ambiguity group locating technique is developed to address the ambiguity problem. Deviations can be accurately computed and fault location is computationally efficient.

To decrease complexity and increase accessibility, a large scale system is decomposed into smaller subsystems. A restriction on accessibility in traditional decomposition is removed, so that some specific inaccessible nodes can be computed for their nodal voltages.

An ideal switch is used to model catastrophic faults. To locate multiple analog catastrophic faults, an analog stuck fault location approach is designed eliminating repetitive simulation requirement among traditional stuck fault location techniques.

The significance of the dissertation research is that efficient and systematic solutions are provided for analog test and multiple fault diagnosis, which are applicable to the general background analog systems.

Approved: _____

Signature of Director