MIXED-SIGNAL TESTING OF INTEGRATED ANALOG CIRCUITS AND ELECTRONIC MODULES

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THIS DISSERTATION ENTITLED

MIXED-SIGNAL TESTING OF INTEGRATED ANALOG CIRCUITS AND ELECTRONIC MODULES

by Zhi-Hong Liu

Has been approved

for the school of Electrical Engineering and Computer Science
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Abstract

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Mixed-signal Testing of Integrated Analog circuits and modules (143pp.)

This dissertation has discussed means and techniques to improve mixed-signal testing of analog integrated systems in industrial environment. It covers a number of practical techniques ranging from component verification, statistical fault detection, and optimum test point selection to innovative use of IEEE boundary scan techniques.

A method to perform the equivalent of In-Circuit Test (ICT) as part of the End-Of-Line Test during manufacturing of modules has been investigated. The experiments have proved that the ICT stage in a manufacturing line can be effectively eliminated for certain modules. This is important as future modules are expected to pose access problems for ICT probes.

A procedure to test analog circuit using the Mahalanobis Distance (MD) is proposed. The proposed methods can be automated in performing fault simulation and in construction of the fault dictionary. It provides a robust statistical model for fault detection with good separation property and simplified representation. The frequency application uses a proper metric to measure the characteristics of analog frequency response. The AR model in the time domain essentially accomplishes a frequency sweep up to two times the sampling frequency. It also reduced the dimension of the MD measures.

A fast algorithm for test point selection is proposed. The proposed approach is based on the entropy measure. It provides an algorithm faster than previously developed

approaches and has fewer selected nodes than most of them. The selection method is applicable for other applications, in which a quality of selection can be established using system entropy, for instance in information systems.

The feasibility study of using digital sequence in analog components testing has been conducted. The analog information can be stored in a sequential digital registers and be shifted out for evaluation. The proposed methodology has special practical value in testing those limited analog components on PCB board along with IEEE std. 1149.1.

Finally, an analog boundary scan bus (ABSB) has been proposed for observing analog function blocks. The proposed ABSB can be used as a subset of IEEE P1149.4 for virtual probe. The proposed ABSB is compared with IEEE P1149.4 by simulation examples. It is concluded that boundary scan bus has its limitation for high frequency applications.

Approved:_____
Signature of Director

Acknowledgment

When I was pursuing my MS Degree in Electrical Engineering in the early 80s at Beijing University of Posts and Telecommunications, my immediate advisor, professor Renheng Tang introduced me the field of analog fault diagnosis and I finished my master thesis in this field. After five years of teaching and working in the telecommunication area, I switched back to the same area for my Ph.D degree in 1990 at Ohio University. It is impossible for me to come to the states without Dr. Januzs Starzyk, who offered me a research assistant position at Ohio University.

Thanks to Dr. starzyk, Dr. Susana Stoica, and Mr. Gary Mazynski, I got a chance to work in Ford Motor Company in the area of manufacturing testing. My experience at Ford is essential to the selection of the topics, which emphasized more on the application of theory to industry. During my work in Ford Electronics (Now Visteon), I learned a lot from Mr. Lawrence Kirk in the understanding of electronic design and analog integrated circuits and from Dr. stoica in the understanding of basic test concepts. I also got technical guidance from Dr. Dan Dandapani from University of Colorado at Colorado springs. The strong leadership from Dr. Depak Goel and Dr. Stoica helped our project and my dissertation.

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List of Abbreviations

ABS. . . . . Antilock Brake System

ABSB . . . . . Analog Boundary Scan Bus

AI. . . . . Artificial Intelligence

AMS. . . . . Analog and Mixed-Signal

AR. . . . . Autoregressive

ARMA. . . . . Autoregressive Moving Average

ASIC. . . . . Application Specific Integrated Circuit

ATE. . . . . Automatic Test Equipment

ATDI. . . . . Analog Test Data In

ATDO. . . . . Analog Test Data Out

BILBO. . . . . Built-in Logic Block Observer

BIST. . . . . Built-in Self Test

BSD. . . . . Boundary Scan Design.

CUT. . . . . Circuit Under Test

CV. . . . . Component Verification

DC. . . . . Direct Current

DFT. . . . . Design for Testability

DR. . . . . Data Register

DSP. . . . . Digital Signal Processing

DV. . . . . Design Verification

ED . . . . . Euclidean distance

EMC. . . . . Electromagnetic Compatibility

EOL. . . . . End-Of-Line

FFT. . . . . Fast Fourier Transformation

FSM. . . . . Finite State Machine

IC. . . . . Integrated Circuit

ICT. . . . . .In-Circuit Testing

IR. . . . . Instruction Register

JETAG (JTAG). . . . . Joint European Test Action Group

LFSR. . . . . Linear Feedback Shift Register

LSSD. . . . . Level Sensitive Scan Design

MA. . . . . Moving Average

MCM. . . . . Multi-Chip Modules

MD. . . . . Mahalanobis Distance

PCB. . . . .Printed Circuit Board

PAM. . . . . ..Pulse Amplitude Modulation

PPM. . . . . parts per millions

PWM. . . . . ..Pulse Width Modulation

PRSG. . . . . Pseudo Random Signal Generator

PSD . . . . . Power Spectrum Density

PWB. . . . . Printed Wire Board

R&D. . . . . Research and Development

RF. . . . . Radio Frequency

SAT . . . . . Simulation After Test

SBT . . . . . Simulation Before Test

SMD . . . . . Surface - Mount Devices

TAB. . . . . Tape-Automated Bonding

TAP. . . . . Test Access Port

TCK. . . . . .Test Clock Input

TDI. . . . . .Test Data Input

TDO. . . . . Test Data Output

TMS. . . . . Test Mode Select

TRST. . . . . Test Reset Signal

Chapter 1 Introduction

Electronic applications have become ubiquitous in industry, science, and everyday life. As modern applications demand greater complexity and smaller packaging, testing will be even more critical. But by the nature of this evolution the methodologies for testing in turn become a greater challenge.

Contemporary technological trends in the electronics industry include surface-mount devices (SMD), tape-automated bonding (TAB), miniaturized components, multi-chip modules (MCM), and application specific integrated circuits (ASIC).

When electronic testing is used in industry it can have numerous benefits. It assures product quality when implemented during key phases of product development. It provides an effective method for concept proving, design validating, and process checking. It also serves as a major determining factor in product time-to-market.

Electronic tests are system-dependent and are classified as either digital, analog, or mixed-signal. Current methodologies for the testing of digital circuits are well-developed. These include D-Algorithm [AIR83], Level Sensitive Scan Design (LSSD) [EIC77], IEEE Standard 1149.1, and Built-in Logic Block Observer (BILBO) [KOE79].

By contrast, methodologies for the testing of analog circuits remain relatively underdeveloped due to the complex nature of analog signals. Present strategy in industry is "to make analog periphery very, very small " [DES93]. But if the applications in digital electronics are so successful and dominant, then why is there still a need to study analog and mixed-signal testing? Stated simply, analog circuitry is where the digital and analog worlds

meet.

In a primarily digital system, analog circuitry is where speech signals are converted to digital signals, sensor signals are conditioned into microprocessors, digital bit streams are converted to RF (Radio Frequency) modulation patterns or horizontal scan lines on a computer graphics screen, and microprocessors send control signals to actuators.

Even with a pure digital board there still exist power supplies, pull-up resistors to do level shifting, and capacitors for EMC (Electromagnetic Compatibility) testing. All of these discrete components on a board need to be tested in manufacturing and "when digital clock rates get really high, the 0's and 1's don't have real meaning anymore. The behavior is essentially analog." [DES93] Therefore the importance of analog testing is increasingly significant.

In addition to pure digital circuitry, analog and mixed-signal (AMS) integrated circuits and modules are widely used nowadays. Integrated circuits (IC) with digital, analog, and mixed-signal circuits on the same substrate are common [ISM94]. The applications for AMS include consumer electronics, wireless communications, networking, multimedia, automotive, process control, and real-time control systems.

With such wide applications, AMS circuits will be the mainstream of future electronics, making it imperative to research AMS testing, including digital and analog testing. But because methodologies for the testing of analog circuits are so far behind their digital counterpart, they become the bottleneck in AMS testing. The objective of this dissertation then is to study AMS testing.

New AMS test methodologies need to be compatible with existing digital testing and

be practical in compromising test coverage and test economics. Therefore basic industry test issues are presented in section 1.1 before the motivation of the main thesis in section 1.2.

1.1 Basic test issues

Any specific test method is only suitable in a particular case. To develop the best test strategies, it is necessary to know where, when, and what to test. Let us first address the where-to-test question. Tests can be performed at multiple phases of a product such as in Design Verification (DV), manufacturing, or field services. DV is used in the Research and Development (R&D) phase. Its major function is to check whether the design meets the specification requirements under all possible application conditions (such as temperature, humidity, component variations, etc.). Manufacturing testing is used in the production phase. Its function is to check the manufacturing process so that the faulty modules are rejected. In the field and service phase, testing is needed to provide satisfactory services to the customers by locating faults and replacing the faulty components with good ones as soon as possible.

Different test strategies are used in the three product phases, but the best practice is to have a unified methodology which can be used throughout the life of a product. This can be achieved by following the Design for Testability (DFT) guidelines (i.e. the IEEE standard 1149.1 [IEEE1990]). While DFT is mainly used in manufacturing testing to replace In-Circuit Testing (ICT), DFT can also be used in other phases.

When to test is critically important to test economics. Electronic tests can be performed at several levels including wafer level, package level, module level, system level,

even in the field service level. The actual cost for the manufacturer at each level roughly follows the multiple of ten rule. For example, the approximate cost for a company in detecting a fault is one to ten cents at the wafer level, ten cents to a dollar at the package level, one to ten dollars at the board level, ten to a hundred dollars at the system level, and one hundred to one thousand dollars in the field service level respectively [WIL86]. Therefore, a fault should be detected as early as possible. Even though it is better to find a fault earlier, some later process changes may introduce additional failures. Therefore, an optimization of testing effort or some compromise should be incorporated in the test procedures.

What faults to test question addresses various categories of test procedures. Tests can be classified into fault detection, fault location, or fault prediction. In the manufacturing process or during maintenance, a quick check is needed to pass the good parts and reject the bad parts for maximum product throughput. So, only fault detection is needed to evidence the faults. At other times, fault location is needed to detect failed modules or components for repair. The faulty components may be a functional block, a failed module, or a failed component. Fault prediction is used mainly with highly reliable products or safety related products (i.e. in avionics and antilock brake system (ABS) modules in automobiles). Fault prediction continuously monitors the circuit under test (CUT) to identify whether any of the its elements are about to fail allowing for a preventive repair.

The choice between fault location and fault detection creates compromises to be made. Fault location needs better isolation of the components and provides better test coverage. It may be used at both assembly lines and repair stations, but it may slow down the

testing process and the throughput. One must keep in mind that the purpose of testing is to help improve product quality. If a manufacturing process has good parts with a low PPM (parts per millions) defect rate, only fault detection is needed and the faulty products can be sent to the repair station or thrown away depending on the repair cost. If a manufacturing process has poor performance and a high PPM defect rate, it is too expensive for the manufacturer to throw away the faulty parts. In order to repair them, fault location is needed. The IEEE 1149.1 standard can provide a decent fault isolation. But for mixed-signal testing, the proposed IEEE P1149.4 standard is still not widely used. In order to locate every fault, most nodes need to be accessed in the network, a requirement which may be impossible to meet in modern fabrication process.

What to test also addresses the types of tested circuits. This includes testing of IC chips and the PCB (Printed Circuit Board). Testing of a chip includes checks for manufacturing defects like layer-to-layer shorts, discontinuous wires, and thin-oxide shorts to the substrate or the well. Testing of a PCB involves testing for manufacturing process defects, component defects, and solder defects. The process defects include wrong, missing, reversed, misplaced parts as well as SMD on edge, SMD tombstone, SMD extra placement, SMD inversed part, and the process damage. The component defects include poor soldering, defective parts, open PWB (Printed Wire Board) traces, and IC lead coplan. Manufacturing defects include no solder, insufficient solder, solder balls, solder voids, excess solder, and shorts. The following classifies the faults.

Classification of Faults

- Deviation Faults - those which deviate from acceptable values of the parameters in a continuous manner into unacceptable value ranges
- Catastrophic Faults - those which refer to sudden or large variations of the parameters, e.g. short and open.
- Single or Multiple Faults - single faults pertain to only one parameter at a time, while multiple faults relate to several parameters or components simultaneously

The current approach to detect manufacturing faults in today's PCB industry uses several forms of Automatic Test Equipment (ATE): bare-board testers, ICT testers, and functional testers. After fabrication of a raw unassembled board, bare-board testing is done for open-etch circuits between nodes by forcing a voltage onto one circuit node and sensing the voltage at other circuit nodes. After board assembly, the ICT is done to check for part orientation, part value, part type, and correct solder joints between all parts on the PCB. Software models of each part on a board are used to generate the test patterns used by the in-circuit tester. The main assumption is that both the board and in-circuit testers require physical access to nodes or points on the board in order to perform the necessary testing. A functional tester is usually customized to a particular product. The test is performed after packaging the product to check the functionality of the product. Usually, it tests the circuit through edge-connectors. Both bare-board and in-circuit testers require the ability to inject a voltage or current onto a network and sense the voltage or current at another point on the network. But the shrinkage in dimension of PCB board and the application of SMDs make

it impossible to access every test point by an in-circuit tester. Therefore, alternative methods must be found to address these challenges. IEEE standard 1149.1 [IEEE90] and IEEE proposed standard P1149.4 [IEEE96] are such alternatives which provide virtual probes. With more and more functions integrated into chips, PCBs tend to have simple structures. A typical configuration has the microprocessor in the center and all input-output circuits in the peripheries. In Section 3.1, a component verification approach is described to test such simple modules through edge connectors.

By now, new microprocessors and ASIC start to incorporate boundary scan designs (BSD). BSD is a structured test technique where shift registers and latches are placed at the functional I/Os (Input/Output) of an IC. Each I/O pin can be driven to a known state or its current logic level can be captured and scanned out via a proposed four-wire serial bus. The test bus and protocol as well as the behavior of the boundary cells are defined in IEEE Standard 1149.1. BSD was developed to test IC interconnects on PWBs when physical access test points are impossible, difficult, or impractical. As the IC pin counts increase, pin spacing decreases, and pin accessibility disappears, therefore BSD is playing an increasingly important role in design verification and manufacturing.

BSD must be optimally designed to maximize the benefits of its use. There are usually many factors that determine to what degree the BSD is needed on a PWB. Lack of physical access is the number one reason to use BSD regardless of the cost/benefit tradeoff. Test development time and costs as well as fault isolation requirements justify the cost of adding the BSD. Test equipment costs and test execution time also help to justify the added cost of BSD. On the other hand, BSD is not cost effective for some consumer products such

as automotive applications, where even one dollar increase per module adds up to a huge sum of money because of the production volume. In this case, the benefits of BSD can only be realized by considering time-to-market, customer satisfaction, and system integration. For an end product such as an automobile, subsystem manufacturers are known as suppliers. For a subsystem manufacturer, module manufacturers are suppliers. For a module manufacturer, chip manufacturers are suppliers. The business relationship between assemblers and suppliers is one where both parties need to profit. The buyers need to buy cheaper while the suppliers tend to sell expensive. So, it is very hard to justify the cost effectiveness of BSD from a single manufacturer. In order to utilize BSD in every stage of the product, collaborations between different parties are needed. Therefore, the primary driving force behind BSD is a reduced time-to-market it offers. If automobile manufacturers shorten their design cycle to a certain number of months (currently 15 to 24 months), the suppliers have to choose BSD to meet the deadlines.

The secondary purpose for using BSD is customer satisfaction. If automobile owners require time-sensitive repairs, the suppliers have to use the BSD.

The third reason for using BSD is system integration. If manufacturers and suppliers consider themselves as one unit, some compromise can be achieved to solve the cost problems.

In the above section, some basic test issues are summarized and modern trends in testing are discussed. In the following section the research topics addressed in this dissertation will be introduced.

1.2 Introduction of the dissertation topics

The objective of this dissertation is to improve mixed-signal testing of analog integrated circuits and modules under constraints of manufacturing industries. These constraints include testing cost and reliability, testing time and accessability of tested components, as well as IEEE standards and industrial practices. In particular, two major topics are researched -testing strategies in mixed-signal circuits which include test point selection and the innovative use of boundary scan techniques for both digital and analog circuits to improve mixed-signal testing. Motivation for this work was driven by author's involvement in research and testing work at automotive microelectronic industry.

Electronic Testing is beneficial for detecting defects and assuring quality, but it impacts production costs and time-to-market. A favorable solution is to have one methodology which can be reused in testing chips, modules, and systems.

IEEE boundary scan standard provides such methodology but the additional cost of its integration may not be seen as offsetting its benefit. The inaccessibility of test nodes and lengthened development lead time are major concerns, and in analog and mixed-signal testing those concerns are heightened.

Some of the difficulties in analog testing include spawn from the analog signal inherent nonlinear property, the lack of proper fault models, susceptibility to distortion, measurement errors, and node inaccessibility. Analog testing has become the bottleneck of mixed-signal testing, and analog diagnosis is reviewed in Section 2.0.

Since large analog circuits are cumbersome to test it is necessary to divide the

network into smaller sub-networks. The network can be partitioned according to circuit functionality, macro cells, or test algorithms which have been developed for optimum test point selection. Three approaches to analog test strategies are discussed in chapter 3. In the first two approaches, it is assumed that a partition has been made, while the third approach tries to find the best partition.

The first approach, component verification (CV), is geared toward the manufacturing testing of a special family of PCB boards used in automotive and computer peripherals. The modules have a simple circuit structure and are produced in large quantities. It is not cost effective to apply IEEE 1149.1 or IEEE P1149.4 to these PCB boards, thus a single station replacing current ICT test and functional testing is suggested. Based on computer simulations and component tolerances, the CV approach through edge connectors can be implemented. To ensure fault detection, a corresponding testability measure based on sensitivity analysis is used. It can be implemented in the design stage as additional restraints and DFT guidelines. A special methodology to measure and calculate pull up circuitry will be discussed as an example. In the first approach, test nodes are selected through edge connectors and test frequencies are selected heuristically. The test limits are checked in several frequencies. To increase test resolution, combined test limits from various frequencies are used.

To provide a single metric for multifrequency test, the second approach uses Mahalanobis Distance (MD) criteria. MD method is used in pattern recognition and it also can be used in fault diagnosis or fault detection. It is the expansion of the first approach and superior to the simple CV approach. MD measures can be used in the domains of both

frequency and time. However, the application of MD in frequency domain does not provide a method to determine optimal test points, thus various simulations must be performed.

Another way to determine optimal test points is an information-based approach which will be explored in section 3.3. The time-domain approach of MD measures is a way of avoiding test point selection. In this approach, a digital signal processing (DSP) based scheme is suggested. The ARMA (autoregressive moving average) parameters are solved using sampled discrete points. This is essentially equivalent to frequency sweep instead of a few selected frequencies depending on sampling rate. The MD measure of AR (Autoregressive) parameters are then used. The proposed method is as suitable in both manufacturing testing as it is in on-line testing. The advantage of using the MD in time domain is improved selection of time and frequency measurements. The proposed method is generic and has been programmed into SABER software package.

The third approach is information based, which is an excellent method for test-point selection in decision-table applications. Rough set theory is also used for better understanding of the problem. The effectiveness of such an approach has been proven through computer simulation with 200 randomly selected matrices.

The modern trend in testing is to use boundary scan and DFT methodologies. In Section 4, mixed-signal testing and boundary scan tests are studied. The background and brief description and the IEEE Standard 1149.1 are presented first. Numerical equations are then developed to determine if delay information can be used to verify analog components. The analytical equations for the first order charge/discharge equations are later

derived as the guideline for waveform design.

Analog component testing with the IEEE standard 1149.1 is discussed in Section 4.3. By selecting the correct pulse-train clock and duty cycles, proper 1 and 0 sequences can be observed. The most attractive method is to use input from a pseudo random signal generator (PRSG). This would provide an application for the completely digital testing of mixed-signal systems.

By the end of Section 4, an analog boundary scan bus (ABSB) and virtual probe test bus for mixed-signal testing is proposed. The IEEE P1149.4 boundary scan test bus is also discussed. The boundary scan test fixtures can be used in both chip fabrication and board manufacturing. Considering the contemporary use of cell-based designs, how to test analog cells or macro cells more effectively is sometimes more important than the circuit partition. The limitation of IEEE 1149.4 is also presented by computer simulation. Simulation results are provided in each chapter.

Chapter 2 A Review of Analog testing

Mixed-signal testing includes analog and digital testing. In digital testing, the fault models are clearly defined by stuck-at-fault [ABR90], and the scanning and storage of digital signals are easily accomplished by using shift registers. As a result, the IEEE Standard 1149.1 is a very successful DFT strategy. However in analog testing, there is no such effective methodology. The analog fault model is not clearly defined, the scanning and storage of analog signals are almost impossible, and the IEEE Proposed Standard P1149.4 is far from practical for most applications. Therefore, the bottleneck of mixed-signal testing is analog testing. It is necessary to review previous works and to find out why it is difficult to perform mixed-signal testing, what has been previously done, and what can be done in the future.

Analog fault diagnosis has been researched for more than 30 years. Even though analog circuits came into existence well before the advent of digital circuits, the development of analog testing can not match its digital counterpart. One reason is the lack of proper models like stuck-at-zero and stuck-at-one models used in digital testing. The nonlinearity, the continuous characteristics, the broad range of frequency components, the high sensitivity to loading, the easiness to distort internal signals, and the component tolerances make testing of analog circuits even more difficult.

Two outstanding reviews of analog diagnosis were presented by P. Duhamel et al. [DUH79] and J. Bandler et al [BAN87]. Duhamel et al. reviewed and assessed the techniques available before 1979 for automatic test generation of analog systems by classifying different

methods and providing an extensive bibliography. Bandler et al. summarized various fault location techniques and algorithms developed before 1987 and added most algorithms developed after 1979. They discussed the fault dictionary approach, the parameter identification approach, the fault verification approach, and the approximation approach. Two books covered representative methodologies in analog fault diagnosis [LIU91] and modern approaches to mixed-signal testing [VIN98]

The measures of testability and the degree of algorithm complexity are the basic theoretical topics for fault diagnosis. The testability studies tell whether the CUT is testable or not for a given methodology, while the degree of complexity tells the effectiveness of the proposed algorithm. Both are related to the specific algorithms and the ways the test equations are formulated. Their effectiveness relates to the kind of faults being targeted. The testability measures can be defined in DC, frequency domain, and time domain.

Analog circuit diagnosis methods are generally classified into simulation after test (SAT) and simulation before test (SBT) [DUH79][BAN85]. SAT methods focus on parameter identification and fault verification and they are very efficient for soft faults diagnosis because they are based on a linearized network model. However, the major problem in parameter identification is the ability to access test points. Very often, there are not enough test points to test all components or each added test point is too expensive to accept. As an alternative, the fault verification method addresses the problem of limited number of measurements, in which, not all parameters of the circuit can be identified at a time. This method assumes that only a few components are faulty and the rest of the network components are within design tolerances.

Faulty components are identified by checking the consistency of certain network equations. The ability to test multiple faults is limited by large number of choices of faulty components, which result in the combinatorial explosion for large designs. The SAT approaches have the disadvantage of high on-line computational complexity, inability to deal with catastrophic faults with ease, error prone to component tolerances, and high numerical sensitivity. To compromise test coverage and test simulation, SBT methods emphasize on building a fault dictionary in which the nominal circuit behaviors in DC, frequency, or time domain are stored. In the test stage, the measured circuit behavior is compared with the nominal case and the faults are diagnosed. In manufacturing testing, a DC test is reliable and effective. However, when higher test coverage is needed, a frequency test or a time domain test may provide more information about the circuit under test without adding test nodes. In the following sections, two most representative methods in SAT namely parameter identification and fault verification are discussed. This is followed by discussion of the SBT methods.

2.1 SAT methods

The first task of parameter identification technique is to formulate a sufficient number of independent equations from the measurements to determine all component values. A component value that lies outside the design tolerance range specification is identified as a faulty component.

R.S. Berkowitz [BER62] introduced the concept of network-element-value solvability

by presenting the necessary conditions for passive networks in 1962. Even without an algorithm, Berkowitz's studies heralded a new research area, analog fault diagnosis. Saeks et al. [SAE72] proposed a method to determine parameter values using voltage and current measurements, when a single excitation is applied. Multiple current excitations are applied to a network and voltage measurements are used to identify network parameters by Biernacki and Bandler [BIE80a]. Biernacki and Starzyk [BIE80b] gave test conditions which are sufficient conditions for network solvability problems. T.N. Tricks et al. [TRI79] researched the necessary and sufficient test conditions for a single test frequency and introduced the adjoint circuit concept into fault diagnosis. In Tricks's study, the branch voltages of the unknown components should be available so that the components can easily be solved by a linear method. N. Navid and A. N. Willson [NAV79] have given the necessary and sufficient conditions for the element-value solvability of a linear resistive network. They show that one can determine if it is possible to compute the element values from the test terminals by considering only the circuit's topology. Ozawa and Kajitani [OZA79] studied the problem of diagnosability of linear active networks using a voltage and current graph. Starzyk et al. [STA84] used Coates graph and presented topological and graph-theoretical conditions to determine the required number of excitations and voltage measurements for evaluation of faulty elements within a sub network. T. Ozawa et al. [OZA83] researched generalized Y-Δ transformation with a voltage controlled current source and its application to element-value solvability problems. The inaccessible nodes in a network are eliminated one by one by the transformation and a sequence of networks are obtained. They researched the backward process of Y-△ transformation to determine the solvability problem. Visvanathan and

Sangiovanni Vincentelli [VIS81] developed a theory for the diagnosability of non-linear circuits with DC inputs. They derived conditions for the local diagnosability and showed that for diagnosable systems, it is possible to obtain a finite number of test inputs that are sufficient to diagnose the system.

All of the methods mentioned above deal with DC domain or single frequency excitation. The multifrequency techniques include research on the test point selection and test frequency selections. R. Saeks [SAE77] introduced a testability measure via multifrequency measurements for linear systems and its applications to test point selection. His approach was further discussed by Sen and Saeks [SEN79], and Chen and Saeks [CHEN79]. Saeks' measure is appealing because it provides a quantitative measure of testability and it results in an efficient computational algorithm. R. Priester et al. [PRI81]] proposed a testability measure based on optimal experiment designs borrowed from system identification theory. Priester's measure provides more information on the degree of difficulties about the testability. Rapisarda and Decarlo [RAP83] proposed the tableau approach with multi-frequency excitation for analog fault diagnosis instead of transfer function oriented algorithms. A. Abderrahman et al. [ABD96] used optimization techniques to generate multifrequency test sets for parametric and catastrophic failures. Sheu and Yuen [SHEU96] proposed an efficient frequency domain relaxation pseudo-circuit approach and the associated solvability conditions with reduced dimension and practical implementation scheme.

The time domain approach includes formulating solvable equations which are testable from time domain measurements. R. Seaks et al [SAE81] published an excellent work on

dynamic testing. They extended their diagnosability theory for linear systems [Sen79] and memoryless nonlinear systems [VIS81] by presenting a necessary and sufficient condition for the local diagnosibility of nonlinear dynamical systems. Based on a discrete-time circuit description, V. Visvanathan [VIS84] derived a necessary and sufficient condition for the local diagnosability of a class of nonlinear dynamical circuits whose branch relations are analytic functions of their argument. H. Dai [DAI90] proposed an efficient approach for functional testing and parameter estimation of analog circuits in time domain based on a sensitivity matrix. Salama and Amer [SAL92] developed a technique based on identifying the discrete time transfer function coefficients of the circuit under test from time domain response. Walker et al. [WAL92] developed a two stage SAT fault diagnosis technique based on bias modulation. The first stage, which diagnosis and isolates faulty network nodes, resembles the node fault location method [HUA83]. The second stage, a sub-network branch diagnosis extracts faulty network parameters. The branch diagnosis is achieved by element modulation, a technique to vary the value of the element externally as a modulated element.

The works discussed so far focused on the parameter identification method. The fault verification methods use almost the same equations as are used in the parameter identification approaches, except that in the fault verification approaches, circuit components are partitioned into two groups, a fault-free group 1 and a faulty group 2. It is assumed that all components in group 1 are fault-free and all faults are localized in group 2. Using the measurement data and the nominal characteristics of all circuit components test equations are formulated and expressed as functions of deviations of group 2 components.

Test equations are overdetermined and can be satisfied only if all faults are indeed localized in group 2. Thus the technique of making assumptions on faults and checking their validity is called fault verification.

Another quantative testability measure which is based on sensitivity was introduced by Temes [TEM77] and was further studied by Dejka [DEJ77]. Skala [SKA80] studied a sensitivity algorithm for checking the consistency or inconsistency of certain linear equations which are invariant on fault elements. H. Dai [DAI90] proposed a testability measure using time domain sensitivity equations. Slamani and Kaminska [SLA92] used sensitivity equations and optimization method for selecting test sets.

From the topology point of view, Z.F. Huang et al. [HUA83] introduced k-node-fault testability in 1983. In their studies, node-voltages and nodal equations are used. The beauty of their testability condition is that it depends only on the graph of the circuit instead of the component values. C.S. Lin et al. [LIN83] studied the topological conditions for single-branch-fault. Maeda et al. [MAE86] presented necessary and sufficient analytical as well as graph theoretic conditions for fault detectability and distinguishability in non-linear systems and used these conditions to derive an algorithm for fault diagnosis. Starzyk and Dai [STA92] presented a decomposition approach for testing large scale analog non-linear networks. This was found to be superior to conventional methods using sensitivity approach.

No matter what kind of testbility measures are used, whether it is frequency domain, time domain, or topology point of view, the advantage is that the measure tells whether the CUT is testable or diagnosable. However the computational complexity is a difficult problem

to overcome. In manufacturing testing, this problem becomes more severe. SBT methods provide a compromise by shifting the computational burden to simulation before test.

2.2 SBT methods

Martens and Dyck [MAR72] used a frequency domain approach for single element faults. They considered a transfer function as a bilinear function of network elements. Morgan and Towill [MOR77] included the higher order harmonics in the dictionary for the frequency domain response of the network. Varghese et al. [VAR79] utilized the Euclidian norm to normalize the network response deviations. Lin and Elcherif [LIN85] considered DC inputs to build the fault dictionary. Seschu and Waxman [SES86] employed a frequency domain approach to construct a fault dictionary of a linear frequency-dependent circuit.

Time-domain analysis approaches were also studied to construct the fault dictionary. Pseudo-noise signal inputs are used by Macelod [MAC73]. For each faulty condition, the deviation in the impulse response of the network is computed using a periodic pseudo-noise signal as excitation. These deviations are quantized and are stored in the dictionary. Schreiber [SCH79] proposed the test signal design method to construct the fault dictionary. In this, the loci of all single-element drift failure fault signatures are drawn in the augmented signal space to generate the fault dictionary. Wang and Schreiber [Wan79] utilized a complementary signal approach for go/no-go testing of a partitioned network under test. Balivada et al. [BAL96] have studied the effects of various stimuli on the variations in delay, rise time, and over shoot that indicate faulty behavior. M.A. AI-Qutayri [AI92] presented a

time-domain go/no-go testing strategy for analog integrated circuit macros. His strategy is based on exciting an analog macro with a pseudo-random binary sequence and measuring the transient response at the external nodes. With an increasing number of macro based designs in application, testing macros becomes attractive and necessary.

Different types of measurements were used in the literature to construct the dictionary. The widely used measurements are node voltage [HOC79][LIN85], magnitude and phase of node voltages [PAW82], and voltage/ current measurements [RUT94]. Power supply current and voltage measurements are also used by Papakostas and Hatzopoulos [PAP94] who suggested power supply current measurements in linear bipolar ICs for fault detection. Somayajula et al. [SOM96] proposed construction of fault dictionaries from the currents in the power supply bus. A ramping power supply is applied at the DC power supply inputs to force the transistors in the circuit to operate in all possible regions. Then, the signatures are clustered into different groups using a Kohenen neural network classifier. Aain et al. [AAI94] suggested testing of analog circuits by power supply voltage control. The power supply voltage was varied and output voltage was measured for the opamp circuits to detect faults, which were otherwise difficult to find with conventional input signal excitation. They also discussed [AAI96] application of AC power supply voltage and compared the fault coverage of voltage level and supply monitoring schemes. In addition, they discussed the effect of changing the power supply frequency on the testing of analog Ics.

Artificial intelligence (AI) and neural network methods and are also used in analog fault diagnosis especially in SBT methodologies [BER96][MAT96][HAT89][MAN90]. Hatzopoulos and Kontoleon [HAT89] proposed a method which provides the knowledge

base to the computer with qualitative and quantitative, nominal and faulty, element models and their possible failure symptoms. Manetti et al. [MAN90] proposed methods to generating methods to generate test point selection using AI techniques, based on a knowledge based constituted by simple rules derived from experience and heuristic reasoning. Based on the back propagation paradigm, several authors studied analog fault diagnosis [RUT94][WU94][YU94] [SPI97]. Rutkowski [RUT94] employed backpropagation network for locating faults in a non-linear dc circuit. Yu et al. [YU94] proposed the neural network approach for the fault diagnosis of CMOS Opamps with gate oxide short faults. In this case neural network is trained to respond for the variations in supply current. Wu and Meador [WU94] suggested a feed forward neural network approach for IC fault diagnosis in a large scale production testing environment. However all these methods present the problem of long training time to converge, even with a relatively small number of training samples.

Probabilistic and statistical techniques were proposed by some authors for analog fault diagnosis [KRA63][PRI81][FAV91][EPS93] [CHA97][DEV96]. Kranton and Libenson [KRA63] developed a probabilistic technique for single faults. In their studies, all possible faults were characterized statistically using Monte Carlo simulation and stored as a data base similar to fault dictionary. At the time of testing, the probability for each individual element to be faulty was computed using a limited number of measurement and the stored data base. Epstein et al.[EPS93] presented statistical techniques using discrimination analysis and hypothesis testing for fault detection and classification in linear integrated circuits. Favalli et al [FAV91] presented a probabilistic approach to detect analog faults that depends on the conductances of faulty and fault-free networks. Using this they gave methods to find

detection probability of each fault and the expected coverage of analog faults. Gielen et al [GIE96] suggested to use A-priori simulated probability information combined with actual measurement data to decide whether the circuit was faulty or not.

The research results discussed provide theoretical basis for analog fault diagnosis. The basic idea of analog fault diagnosis is to formulate equations based on circuit topology and voltage/current measurements so that the desired testability is reached. Unfortunately, most algorithms can not avoid the computational complexity problem, therefore they are rarely used in practice. The most practical methods in analog fault diagnosis are simulation and the fault dictionary approach.

A fault dictionary constructs a look up table, which lists each faulty case and nominal case for comparison purpose. The objectives of fault detection or diagnosis must be clear because they are critical aspects for deciding the fault detection or diagnosis capability of the dictionary. They also have an impact on the size of the dictionary and impose a limitation on the dictionary approach. Too broad fault coverage may end up with prohibitive large number of combinations which may not be realized algorithmically, while too narrow fault coverage may not meet the quality target. The anticipated faults and the nominal circuit of the CUT need to be simulated in order to develop sets of stimuli and responses to detect and isolate the faults. To generate a reasonable fault list, physical failures and failure modes have to be related. In order to develop a fault dictionary with real physical meaning, failure modes and physical failures are discussed in the following section.

2.3 Failure Modes and Mechanisms for electronic components

In constructing a fault dictionary, fault simulation is widely used in choosing the test strategy. Some methodologies use schematics as the starting point to generate fault lists in fault simulation. For example, when a fault list is generated, every component is either shorted, opened, shorted to power, shorted to ground in single fault situation, or a large number of different fault combinations are considered in multiple fault cases. The disadvantage of doing so is that it neglects the physical layout information of the circuitry and hence it could generate some unrealistic faults in the lists or a prohibitively large fault lists. Therefore, very often a single fault assumption is made. Unfortunately such assumption is often invalid. For instance, a single cut line across a PCB generates multiple faults. The drawback of schematic based fault list generation without layout, material, and process information is that some of the faults generated are not likely to exist in the real world. Therefore, simulation time and effort are wasted. Another problem in schematic based fault generation without layout information is its inaccuracy in fault models. For example, in CMOS short circuit simulation, a short between nodes should be a proper resistor between nodes instead of zero resistance [WAL86], especially in an integrated circuit [HAR94] [OLB96]. Therefore, it is advantageous to study testing by relating the system specifications to details of the layout and process. It is necessary to investigate correlations between fault models and physical failures. Based on the probability of the occurrence of physical failures and the fault behaviors caused by such failures, a realistic fault list can be generated and the fault models can then be built. In what follows, failure mechanisms with electrical behavior and fault models for simulation are discussed.

Let us look at failure modes and mechanism first. A failure mode is the effect by which a failure is observed, while a failure mechanism is the chemical, physical, or metallurgical process which leads to component failure [JEN95]. In electronic components, there are basically different failure modes namely, open circuit, short circuit, degraded performance, and functional failures. The relative occurrence of failure modes in some electronic components were summarized by A. Birolini [BIR94] as shown in Table 2.3.1.

Table 2.3.1 Relative occurrences of failure modes in some electronic components [BIR94]

Components	**Short %**	**Open %**	**Degradation %**	**Functional %**
Digital, bipolar ICs	30	30	10	30
Digital MOS ICs	20	10	30	40
Linear ICs	30	10	10	50
Bipolar transistors	70	20	10	--
Field-effect transistors	80	10	10	--
Diodes, general purpose	70	30	--	--
Zener	60	30	10	--
HF	80	20	--	--
SCRs	20	20	60	--
Optoelectronic devices	10	50	40	--
Resistors, fixed	-	90	10	--
Variable	-	60	20	20

Components	Short %	Open %	Degradation %	Functional %
Capacitors, foil	80	10	10	--
Metal foil	40	60	--	--
Ceramic	50	40	10	--
Tantalum, dry	60	20	20	--
Aluminum, wet	20	10	70	--
Coils	10	30	--	60
Relays	15	15	--	70
Crystals	-	80	20	--

Table 2.3.1 shows that most physical failures are open and short faults which are comparatively easier to detect than degradation and functional faults. In PCBs, approximately 75% percent of faults occur at assembly, only 20% percent are component faults, and 5% are PCB faults [Lan88]. An important application of Table 2.3.1 is to calculate test coverage and yield estimation. For instance, if the open fault for a fixed resistor can be detected, 90% test coverage for that resistor is estimated.

In addition to component failures summarized in Table 2.3.1, the failures caused by the manufacturing process are the other important factors. Table 2.3.2 shows the relative percentage of occurrence for a particular manufacturer in its process defects, component defects, and solder defects respectively.

Table 2.3.2 Relative indexes of manufacturing process defects for a manufacturer

Process Defects	**%**	**failure mode**
Wrong parts	10	v
missing parts	7	open
Misplaced parts	7	reliability
SMD on edge	7	reliability
process damage	3	op/sh/v
SMD tombstone	3	op
SMD extra placement	3	leakage
Reversed part	3	v/op/sh
SMD inverse parts	2	v/op/sh/r
Solder Defects		
No solder	7	op
insufficient solder	7	resistive op
Solder balls	7	sh
Solder voids	7	resistive
Excess solder	3	sh
solder short	2	sh
Components Defects		
Poor Sold wet	10	resistive sh
Defective part	7	op/sh/v
open PWB track	3	op
IC lead coplan	2	op
Where v=variable resistance or functional degradation, Sh=short, op=open, and r=reliability		

The actual percentages differ from manufacturer to manufacturer depending on the technology and manufacturing process. For each manufacturer, a table similar to Table 2.3.2 can be used as the reference for deciding the test strategy. More importantly, these figures can be used for finding problems in the manufacturing process. For instance, if one defect occurs more frequently than others, the root cause should be found and process must be improved to reduce the defect rate. As is shown, the failure mode for the listed physical failures can be used to generate a fault list in simulation. In most cases, the faulty behavior of the circuit is caused by open or short. For the wrong parts and misplaced parts which are caused by loading the wrong reel, the failure mode can be open, short, or functional degradation. However, if misplaced parts are to be detected in a ICT or a functional tester, it is too late, because ICT test is after assembly and functional test is after package. Therefore, there may be hundreds of failed parts in the assembly line. As a result, it is better to avoid these faults by bar coding the reels so that each time a reel is loaded, the bar code for the reel is checked first. In summary, the faults can be modeled as open, short, and variable component values. However component value changes are usually significant in these failure modes. As a result, a faulty value with a value ten times larger or ten times smaller is a reasonable assumption in generating the fault list. Open and short faults are only the extreme cases of these two. Therefore, if ten times larger or ten times smaller faults can be covered, the open and short faults can be detected also. Table 2.3.2 address the manufacturing process of PCBs. In what follows, integrated circuits (IC) are discussed.

In an integrated circuit, the failures could be caused by substrate, oxide, metallization,

interconnections, package, overstress [FAN85]. Table 2.3.3 shows the percentage incidence of failure allocation for several IC manufacturers.

Table 2.3.3 Percentage incidences of failure allocations

Failures	Bell TTL	Bell CMOS	Bell MOS	USAF TTL
Substrate	-			4
Oxide	20	1	75	27
Metallisation	30	34		4
Interconnections	37	5	7	9
Package	-	-		15
Not identified	9		1	17
Overstress	4	60	17	24

As is shown, the failure allocation depends on technology and process. It also varies from manufacturer to manufacturer. A refined scheme is shown in Table 2.3.4. This table lists the defect, the physical failure mechanism, and the electrical effects for each failure location.

Table 2.3.4 IC failures, defects, mechanisms, and electrical failure modes

Location	Defect	Failure mechanism	Electrical failure mode
Substrate	Crystal defect close to junction	High generation-recombination Low-resistance paths (CE pipes) Second breakdown alpha particles	Refresh time degradation in RAMs Leakage/short circuit Short/open circuit Soft errors
Thin Oxides	Traps and charges at Si-SiO2 Interface Oxide traps	 Hot carrier injection and trapping	Leakage/characteristic Instabilities and degradation MOS threshold and tansconductance degradation
Thin and Thick oxides	None Pin-holes Other defects/contaminats Contaminants (alkali ions)	High E-field breakdown (eventually ESD) Low E-field breakdown Time dependent breakdown Surface depletion/inversion	Leakage/short circuit Leakage/short circuit Leakage/short circuit Leakage/characteristic Instabilities and degradation parasitic MOS transistors
Contacts	Surface defects/nonsaturated AI Oxidised surface None	Metal-Si interdiffusion Electromigration	Leakage/short circuit Open circuit/floating conductors Junction leakage/short circuit Metal open circuits
Conductors	Thinging (High steps.scratches) None None Contaminats	Joule melting/electromigration Electromigration Overstress Corrosion	Open circuit Open circuit Short/open circuit (Bridging) Open circuit (AI) Short circuit (Au)
Multilar conductors	AI hillocks	Stress relief/electromigration	Short circuit

Chip-package connection	Poor' wire bonding	Thermal fatigue/mechanical stress	Open circuit
	Excess' wire bonding	Oxide under pad break	Short circuit
		AI particles	
		Au-AI interdiffusion (purple plague)	Open circuit
	Thermal coefficient mismatch between wires and package	Thermal fatique	Open circuit
	Shallow angle of wires with substrate		Short circuit
	Defective die-attach	Poor thermal conductivity thermal runaway	Characteristic degradation
			Short/open circuit

Table 2.3.3 and Table 2.3.4 are used similarly in IC as Table 2.3.1 and 2.3.2 in PCBs. In IC models, short and open should be considered as resistive values according to the technology and process [SAC95]. Failure mechanisms for PCB board and integrated circuits are summarized in this section. The information provided can be used for making test strategy decisions, generating fault lists, and calculating fault coverage in fault simulation. The next chapter will discuss three methods for analog fault diagnosis.

Chapter 3 Analog testing

In this chapter, three test methods are studied. All three methods deal with the fault dictionary approach. The first section discusses combining functional testing and in-circuit-testing into one in manufacturing testing by component verification approach. The second section discusses Mahalanobis distance (MD) and its application to analog fault diagnosis. The proposed MD method can also be used in component verification approach. The third section discusses the reduction of test points using rough set theory and fault-wise table approach.

3.1 PCB board testing using the component verification approach

The PCB boards are divided into two different categories. The first kind of PCBs are the complex ones with the above mentioned components plus additional components. These boards usually require the application of the IEEE boundary scan standards. The second category is systems consist of digital cores surrounded by peripheral analog circuitry, such as filters and data converters. The analog and mixed-signal components serve as interfaces between digital processing circuitry and real world signals. The application of such systems include a board with a micro controller and its input and output circuitry. The exemplary circuitry include most data acquisition boards, engine control modules, automotive body functional control modules, ABS modules, etc. The structure of this kind of PCB board is relatively simple. The application of the proposed IEEE P1149.4 standard not only becomes cost prohibitive but also overkill. These boards are just simple enough to be tested effectively

through edge connectors. The objective of this chapter is to propose a practical method for such systems with minimum test cost.

Most algorithms developed previously utilize ICT to access test points. Many test point selection algorithms were devoted to selecting a minimum set of points. However, future electronic modules are expected to present access problems for the probes in ICT testers. A way around the access problem is to add more access test points on the PCB boards based on current or new algorithms developed. The disadvantage of this is, mathematically, as the test points increase along with the number of components the cost increases as well. This additional cost can be prohibitive. Therefore, the alternative is to use BIST or test electronic modules through edge connectors only. BIST can be realized by using the proposed IEEE P1149.4 standard which is too expensive for low cost electronic modules used in both automotive and consumer electronics where cost is very important for large quantity production. In order to test the module through edge connectors, the circuitry must be simple enough to be traced from each edge connector.

The driving forces for edge connector testing are the need to find an alternative way for manufacturing in-line tests to replace ICTs, the need to have an algorithmic way of generating manufacturing testing programs, and the need to combine ICT and functional tests into one single station. Even if there are only a few test points left inside the PCB board, an ICT is still needed which results in additional testing and higher costs. So, our purpose is to eliminate the need for ICT.

One of the most successful methodologies used in PCB testing is IEEE standard

1149.1. This requires six more pins to be added to the PCB board and each chip in order to implement even the simplest IEEE standard 1149.4 test bus. It is reasonable to add more pins or BIST, if the board to be tested is complex and expensive (say over $1000 per board). However, if the board is simple (say below $100 per board), adding more pins or BIST will significantly increase the board cost so that the IEEE P1149.4 standard could not economically be used. Fortunately, those cheaper boards have simple circuitry and multi-port PCBs. In this case, a technique suitable for PCB testing in data acquisition boards and automotive electronics is studied.

3.1.1 Component verification approach [STO97]

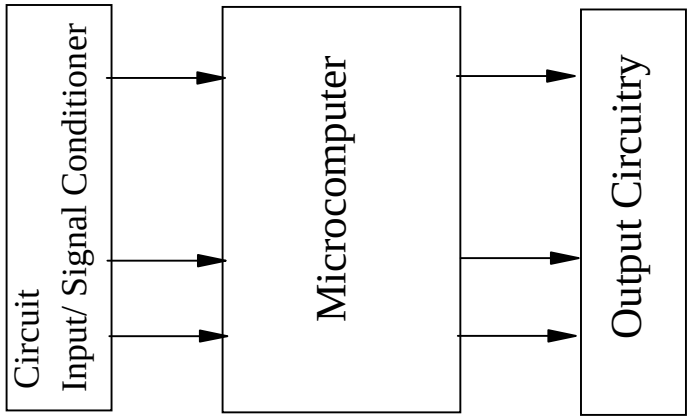

Figure 3.1.1.1 A typical board structure, used especially in automotive

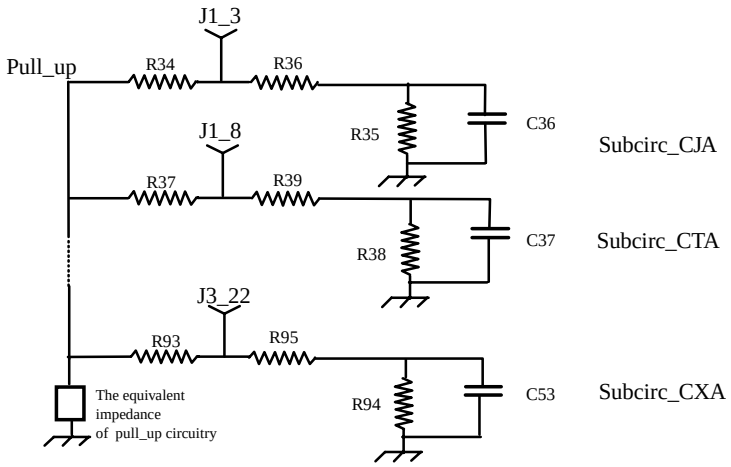

Figure 3.1.1.2 A typical input circuitry

In order to reduce the number of test access points necessary, analog functions are integrated into chips which makes the analog peripheries very small. This is the current trend in electronics. The typical circuit structure is shown in Figure 3.1.1.1 where the micro-controller is in the center of the boards with input circuitry or signal conditioner circuitry and output circuitry at the ends of the boards. The input circuit function is usually used to adjust

the voltage level of the signals from sensors while the output circuitry drives the motors, the solenoids, and the actuators. These input and output circuits are unavoidable in PC based control systems. There are several million boards manufactured each year, thus making it necessary to pay special attention to such systems. Figure 3.1.1.2 shows a typical input network. With this kind of system, it is too expensive to use the IEEE standard P1149.4. Even with IEEE P1149.4, the network from the input pin to the micro-controller pin still needs to be measured by a dedicated circuitry of a chip added to the input pins or by the testers. The question is, do we really need IEEE 1149.4 for this case with the extra 6 to 8 pins? Considering test cost, the answer is probably no. Can we test the network from input pins only and get the same degree of precision? The answer is yes for most cases.

A major contributor to the success of digital testing is that it has a well-defined fault model, such as stack-at-0, and stack-at-1. Analog testing is hindered by the lack of fault models. The reason is because people tried to do too much without simplifying the problems and tried to solve some very hard mathematical problems. Most available testability algorithms are based on calculating the ranks of all possible combinations of linear system equations which make the problem difficult. More importantly all those testability algorithms are concentrated on test point selections which are impossible to use if we want to eliminate ICT. In this section, a method for developing fault model is being researched. Assuming test points are limited to edge connectors, using computer simulation or sensitivity calculations, and considering component tolerances for manufacturing, statistical fault models will be built. The following steps will be used to obtain such models:

Step 1: The circuit test points will be selected from edge connectors.

Step 2: Each test point selected from Step 1 can be classified as input or output. These accessible points can also be considered as multi-port networks. The identified circuits are analyzed using DC, AC, or time domain approaches.

Step 3: For each input pin, test parameters such as voltage, current, or impedance will be obtained. Network parameters such as Z, Y, and A parameters can also be considered, if necessary. Monte Carlo analysis will be used to incorporate tolerance considerations and to obtain the statistical means and deviations for those parameters. Test limits will be obtained by calculating the means and using $\pm 3\sigma$ or $\pm 6\sigma$.

Step 4: Step 3 is repeated with the value of each component being varied by certain amount, say 50% or a value being increased and decreased 10 times each in order to cover manufacturing testing. In the case of transistors, only open and short are considered since we are concentrating on manufacturing tests. i.e. we are verifying soldering defects, processing defects, and components defects. The limits with faults are thus obtained. Comparing the test limits to fault limits, it is possible to decide whether a component is testable or not. If the limits overlap then the component may not be testable. Further analysis is then needed to decide on the testability of the component.

As a case study, let us consider an automotive PCB for body control. Figure 3.1.1.2 shows a typical input circuitry on such a board. The accessible points are input pins such as J1_3 etc. An input impedance analysis is performed. Using the network's impedance, we can make impedance measurements at a minimum of four frequencies, then we can try to solve for the values of those components, provided the circuit is testable under these conditions.

The testability is related to the rank of the Jacobian which relates the derivative of impedance to the parameter values. If all the values are ideal and the circuit is testable, then we obtain a solution. But in this circuit, we have only three independent variables with four parameters to solve. The only solution is to assume that not all of the elements are faulty. We can assume that one element is functional and calculate the other three elements. But in a practical design, we should allow for element tolerances (for instance a 5% change in resistors and a 10% change in capacitors for our components in this circuit). Sometime, we require a 1% resistor change for better resolution designs. The tolerances make the assumption difficult therefore we like to assume that there is only one fault in a sub-circuit.

The symbolic form of the impedance at DC measurement (parameter A) can be expressed as

$$A = \frac{R_{34}(R_{36} + R_{35})}{R_{34} + R_{35} + R_{35}} \qquad (3.1.1.1)$$

The parameters B, C and D can be obtained from the symbolic form of the impedance measured as a function of frequency:

$$|z(j\omega)| = B\sqrt{\frac{\omega^2 + c^2}{\omega^2 + D^2}} \qquad (3.1.1.2)$$

where,

$$B = R_{34}\frac{R_{36}}{R_{34} + R_{36}} \qquad (3.1.1.3)$$

$$C = \frac{R_{34} + R_{35} + R_{36}}{R_{35}(R_{34} + R_{36})C_{36}} \qquad (3.1.1.4)$$

$$D = \frac{R_{36} + R_{35}}{R_{36}R_{35}C_{36}} \qquad (3.1.1.5)$$

The simulation generates random values of all components which are uniformly distributed within the tolerance limits of each component. Then, the means and deviations of those parameters are calculated for three standard deviations to get the test limits for A, B, C, and D's. The test limits are shown in the table 3.1.1.1

Table 3.1.1.1 Impedance test limits for Fig. 3.1.1.2

		A	B	C	D	B-A	D-C
Normal	Min	1766	1718	7172	7387	45	201
	Max	2058	1994	9962	10270	67	320
R34 decreases 50%	Min	892	879	7266	7375	11	102
	Max	1055	1038	10100	10250	18	164
R34 increases 50%	Min	2606	2503	7095	7409	96	292
	Max	3035	2899	9809	10250	143	458
R36 decreases 50%	Min	1731	1607	9781	10560	116	737
	Max	2028	1862	13640	14810	173	1215
R36 increases 50%	Min	1779	1754	6087	6183	23	88

	Max	2088	2053	8823	8962	36	147
R35 decreases 50%	Min	1751	1720	11140	11350	27	194
	Max	2046	2005	16020	16330	43	325
R35 increases 50%	Min	1765	1707	5633	5836	55	190
	Max	2081	2000	8063	8374	85	324
C36 increases 10 times	Min	1762	1716	714	736.5	44	20
	Max	2062	1996	1004	1034	68	32
C36 decreases 10 times	Min	1760	1713	71670	73790	44	1949
	Max	2060	1995	9.87	101800	68	3203

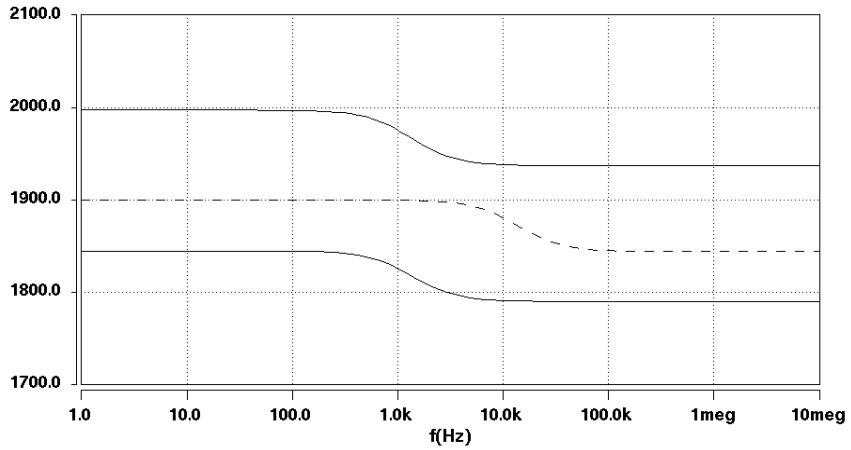

Figure 3.1.1.3. The impedance at pin J1_13

Please note that by measuring B-A and D-C, the testability increased significantly. This can be explained in Figure 3.1.1.3, where the solid lines represent the boundary for nominal case impedance and the dashed line represents a faulty impedance. It can be seen that measuring individual frequency characteristic is not enough to detect such fault. Therefore the values at different frequencies can be combined for making judgement to

obtain a better separation of faults. The effects can be explained in Figure 3.1.1.3. The test limits shown in table 3.1.1.1 was just a sample of the whole test limits for a module. Those limits were programmed into a HP VXI based functional tester which is used for both DV and manufacturing test.

3.1.2 A design for test rule for component verification

The component verification method depends on the visibility of the fault from the edge connectors. In some designs, component values can be manipulated to achieve a better testability design. or at least to improve the test resolution that we can get for the given component tolerances. Let F_k be the kth output variable and ΔF_k be the changes in the output, S^{Fk}_{Xi} be the sensitivity of output F_k versus the parameter x_i and $\Delta x_i/x_i$ be the tolerance of parameter x_i, then we have equation (3.1.2.1)

$$\frac{\Delta F_k}{F_k} = \sum \left| S^{F_k}_{X_i} \right| \frac{\Delta X_i}{X_i} \qquad (3.1.2.1)$$

Without loss of generality, let's assume $\Delta x_i/x_i \geq 0$, we have

$$\left(\frac{\Delta F_k}{F_k}\right)_{\max} = \sum \left| S^{F_k}_{X_i} \right| \frac{\Delta X_i}{X_i} \qquad (3.1.2.2)$$

In order for a ρ percentile change in X_i to be "seen", we assume that $S^{Fk}_{Xi} \geq 0$ and we have,

$$\left(\frac{\Delta F_k}{F_k}\right)_{\min} = -\sum \left| S^{F_k}_{X_i} \right| \frac{\Delta X_i}{X_i} \qquad (3.1.2.3)$$

$$\rho S^{Fk}_{xj} - \sum_{i \neq j} \left| S^{Fk}_{X_i} \right| \frac{\Delta X}{X_i} \geq \sum \left| S^{F_k}_{X_i} \right| \frac{\Delta X_i}{X_i} \qquad (3.1.2.4)$$

After some manipulations, we get,

$$S^{F_k}_{X_j} \geq \frac{2\sum_{i \neq j} \left| S^{F_k}_{X_i} \right| \frac{\Delta X_i}{X_i}}{\rho - \frac{\Delta X_i}{X_i}} \qquad (3.1.2.5)$$

Equation (3.1.2.5) is the guideline for designing a testable circuit for edge connector testing. In order to explain how to use this rule, we look at the Divider design. The divider is shown in Figure 3.1.2.1.

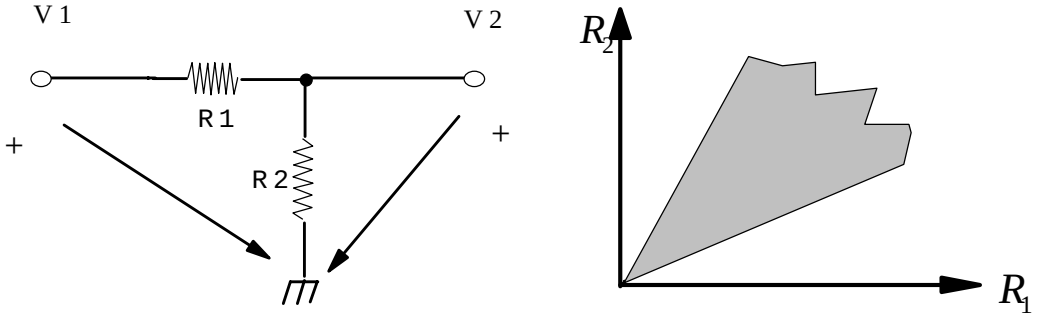

Figure 3.1.2.1 A voltage divider and its feasibility region for testability design

It can be seen that the sensitivities of V_2 versus R_1 and R_2 are the first order partial derivatives taken as $\partial V_2/\partial R_1$ and $\partial V_2/\partial R_2$. Let us assume that we want to detect a 30% error so that $\rho = 0.3$ in (3.1.2.5) and let us assume that the component tolerances are 5% so that $\Delta x_i/x_i = .05$ Substituting ρ and $\Delta x_i/x_i$ into (3.1.2.5), we have $R_2 \geq R_1/2.5$ and $R_1 \geq R_2/2.5$, i.e. $R_1/2.5 \leq R_2 \leq 2.5R_1$. Equation (3.1.2.5) can be considered as additional optimization constraints for component values in the design stage. Figure 3.1.2.1 also shows the R_1 and R_2 region where the shaded area is usable area for the components.

3.1.3 Y-Δ transformation, pull-up resistor measurements, and testability

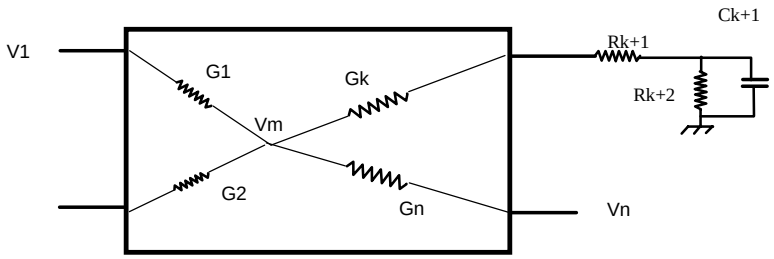

Figure 3.1.3.1 N-port pull-up network

In most applications, pull up resistors are connected to some common regulated voltage sources. A special measurement and calculation methodology is proposed to solve the component values in pull up circuitry. In this method a cluster of components are connected together. We can see that the pull-up resistors of Figure 3.1.2.1 can be separated by measuring the Y parameters of the N-port network given in Figure 3.1.3.1. The Y parameters are defined as:

$$Y_{ij} = \frac{I_j}{V_i}_{|v_i=0(i\neq j)} \qquad (3.1.3.1)$$

Using generalized Y-Delta transformations, the following equation can be obtained

$$G_i G_j = Y_{ij} \sum G_i \qquad (3.1.3.2)$$

Y_i can be measured directly. If we have N input pins sharing the same source, then we have N pull-up resistors. There are N(N-1) Y parameters, so that we have ample equations to solve the above equation to obtain G_i. Once the pull-up values are established, we can apply a DC voltage at any pin, say v_1, and measure the open circuit voltage at each other pins. By Kirchoff's voltage law, we have the following equation:

$$V_m = \frac{\sum G_i V_i}{\sum G_i} \qquad (3.1.3.3)$$

V_m is thus obtained. Since the G_i's are known, $R_{k+1}+R_{k+2}$ can be obtained. By introducing two frequency measurements we can further evaluate R_{k+1}, R_{k+2}, and C_{k+1}.

In summary, section 3.1 studied methods to test a special kind of PCB board which are widely used in automotive and data acquisition boards. The proposed methods test component failures and circuit functions from edge connectors so that ICT and functional test can be combined into a single station. A DFT rule was presented in this section to complimentary the component verification method. The pull up resistor circuitry measurement can be used in some cases. However, some circuitry does not have this kind

of structures. Therefore, these two methods can be used when necessary. In the following section, the Mahalanobis distance measure and its application to testing analog macros are discussed.

3.2 Analog Fault Detection with Mahalanobis Distance (MD)

From the component verification method, the test frequencies have to be carefully selected. For the selected test frequencies, certain patterns should be observed to distinguish the fault from normal cases. To develop a metric for analog fault diagnosis, MD is discussed in this section. From the pattern recognition point of view, MD can be used as the discriminator in fault detection. In section 3.2.1, MD will be briefly reviewed and its applications will be discussed in section 3.2.2 and 3.2.3.

3.2.1 Mahalanobis Distance

To compare and classify different measurement patterns we need to extract their most important features and group the patterns into clusters. Clustering will be based on similarities between patterns and the type of fault each pattern represents. In the problem of feature selection and pattern classification, we are interested in the distance between two multi-variate populations using the means, the variances, and the covariance of the population. The simplest measure of the discriminatory power of a group of features that take into account the correlations between variables is the Mahalanobis distance. For two classes, ω_i and ω_j, and a set of k features, F_1, F_2, ..., F_k, The Mahalanobis Distance (MD) is defined as:

$$D^2(F_1,F_2,...,F_k)=(F_i-\mu_i)^T\sum^{-1}(F_j-\mu_j) \qquad (3.2.1.1)$$

where, $F_i= [x_{i1}, x_{i2}, ..., x_{ik}]^T$ and $\mu_i= [\mu_{i1}, \mu_{i2}, ..., \mu_{ik}]^T$, in which μ_{il} is the mean of lth

feature for class ω_i and Σ denotes the population covariance matrix in which ij-th element is represented by σ_{ij}. The statistical means and variances can be replaced by their estimates $\tilde{\mu}_{il}$, and $\tilde{\sigma}_{ij}$. If the random sample size N yields the sample values x_{1l}, x_{2l}, ..., x_{Nl} for the lth feature, then

$$\hat{\mu}_j = \frac{1}{N}\sum_{i=1}^{N} x_{ij} \qquad (3.2.1.2)$$

$$\hat{\sigma}^2_{jk} = \frac{1}{N-1}\sum_{i=1}^{N} (x_{ij} - \hat{\mu}_j)(x_{ik} - \hat{\mu}_k) \qquad (3.2.1.3)$$

In order to discuss why we use the MD instead of the Euclidean distance (ED), we need to consider that the Euclidean distance attaches equal weight to all the axes of the representation, but in the presence of differential variances and correlations among variate, this may not be a desirable feature. If, for example, variate x_1 has much larger variance then variate x_2 and they are mean-centered and uncorrelated, a scatter plot of a sample of (x_1,x_2) pairs may look like Figure 3.2.1.1.

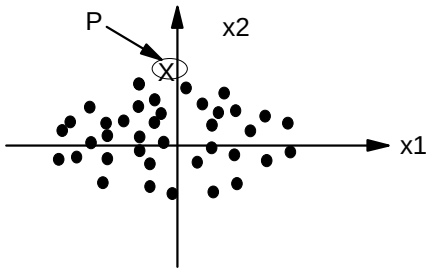

Figure 3.2.1.1 Scatter plot for bivariate

An observation can be much further from the sample mean in the x_1 direction than in the x_2 direction without being necessarily more atypical. The point P looks atypical in the x_2 direction, although its distance from its origin in this direction is less than the distance from the origin in the x_1 direction of many more typical observations. If we now envision two further variate x_3 and x_4 which have similar variances to x_1 and x_2 respectively but are highly correlated, then a large difference in x_3 values between two sample members will be associated with large difference in x_4 values. Thus, in a sense, the Euclidean distance between the corresponding points in the x_3x_4 plane overemphasizes the difference between these sample members. More interest would be attached to a large ED if it were in the x_1x_2 plane, where the variates are uncorrelated and where there is no spurious contribution to the difference between the observations.

Thus, for the ED to be an appropriate measure, the variate used in its computation should be uncorrelated and of equal variance. Given observed variate **x**, let us therefore consider a linear transformation to new variate $\mathbf{y}=\mathbf{Cx}$ in order to satisfy these requirements. If the covariance matrix of **x** is **S**, then the covariance matrix of **y** is $\mathbf{CSC}^T$. Since we want the variate in **y** to be uncorrelated and to have equal variance, we thus need to choose **C** to satisfy $\mathbf{CSC}^T=k\mathbf{I}$ for some k. Without loss of generality, let k=1, we get $\mathbf{S}=(\mathbf{C}^T\mathbf{C})^{-1}$ or $\mathbf{S}^{-1}=\mathbf{C}^T\mathbf{C}$. Now an observed sample member $\mathbf{x_s}$ will have values $\mathbf{y_s}=\mathbf{Cx_s}$ of the new variables, and the sample mean $\bar{\mathbf{x}}$ will be transformed to $\bar{\mathbf{y}}=\mathbf{C}\bar{\mathbf{x}}$. Thus the atypicality d_s of the sth sample member can be measured by the Euclidean distance between $\mathbf{y_s}$ and $\bar{\mathbf{y}}$, i.e.

$$
\begin{aligned}
d_s^2 &= (\boldsymbol{y}_s - \bar{\boldsymbol{y}})^T (\boldsymbol{y}_s - \bar{\boldsymbol{y}}) \\
&= (\boldsymbol{C}\boldsymbol{x}_s - \boldsymbol{C}\bar{\boldsymbol{x}})^T (\boldsymbol{C}\boldsymbol{x}_s - \boldsymbol{C}\bar{\boldsymbol{x}}) \\
&= (\boldsymbol{X}_s - \bar{\boldsymbol{x}})^T \boldsymbol{C}^T \boldsymbol{C} (\boldsymbol{X}_s - \bar{\boldsymbol{x}}) \\
&= (\boldsymbol{X}_s - \bar{\boldsymbol{x}})^T \boldsymbol{S}^{-1} (\boldsymbol{X}_s - \bar{\boldsymbol{x}})
\end{aligned}
\qquad (3.2.1.4)
$$

Viewed in terms of the x variables, this distance d_s is known as the Mahalanobis distance. It is frequently used to measure the distance of a single multivariate observation from the center of the population that the observation comes from. Thus MD can be used to measure the distance of a single multivariate observation from the center of the population that the observation comes from. It is superior over other simple distance measures. For instance the Euclidian distance does not capture correlation between variables and needs to be scaled to reflect differences in variances. Thus MD is more suitable in fault detection where it can provide a good measure of similarity between the observed response pattern and patterns stored in the dictionary. In fault detection only two classes are needed, while in fault isolation many classes may be used depending on how many typical faults need to be isolated. Faulty patterns may be generated by injecting physical failures into the circuit models and performing simulation to determine circuit responses. In the simulation before test process, physical failures are grouped according to their statistical properties expressed by MD measures. In the simulation after test process, the measured waveforms are compared with these groups and their MDs are found to determine whether the circuit is faulty and the physical failures are identified. The advantage of using MD is that a number of features can be used instead of a single feature like one frequency or one sample at a time. The algorithms dealing with fault diagnosis emphasize the frequency selection in the frequency domain and

the decision time in the time domain. Theoretically, time domain and frequency domain testing should be equivalent. However, traditionally, the frequency domain measurements were more stable and easier to control. In the following two sections, The applications of MD are presented. The frequency domain application is discussed in section 3.2.2 and the time domain application with digital signal processing (DSP) is presented in section 3.2.3.

3.2.2 The frequency test and Mahalanobis distance

Frequency domain tests study the circuit behavior at a number of test frequencies. A rule of thumb is to select test frequencies by picking one below the lowest non-zero break point, one above the highest finite break frequency, and one in between. Several test frequencies are needed near break points [SES86].

Some other methods such as QR decomposition [STE87] or fault wise table approaches [BAB97] were studied by researchers. It is not the scope of this section to discuss how to choose the best test frequencies. However, an entropy based approach which can be used for test frequency selection will be studied in the next section. Here, the test frequencies are picked by any available method. The voltage level at each test frequency is considered as one feature in MD measures. Then, the calculated MD in the nominal case and in fault cases are compared to each other to establish the threshold for a decision.

Example 3.2.2.1. The example circuit shown in Fig.3.2.2.1, in which there are 12 resistors with a 5% tolerance and four capacitors with a 10% tolerance. A sine wave was applied at the input and a Saber simulation package was used to get the response measured

at the output. In order to consider component tolerance, 200 Monte Carlo runs were simulated. Each component was failed one by one. The resistor faults were simulated by either letting the resistance equal to 0.1 mΩ to represent a short or letting the resistance equal to 10 MΩ to represent open faults. The capacitor faults were simulated by changing the capacitor value to 1nF and 100nF from its nominal value, 10nF. The frequency sweep response from 1Hz to 10 MHz for the nominal case and R5 open and short faults at V_{11} were shown in Fig.3.2.2.2.

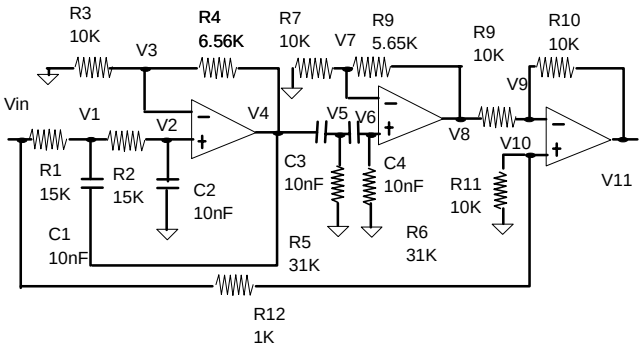

Fig. 3.2.2.1 An active filter

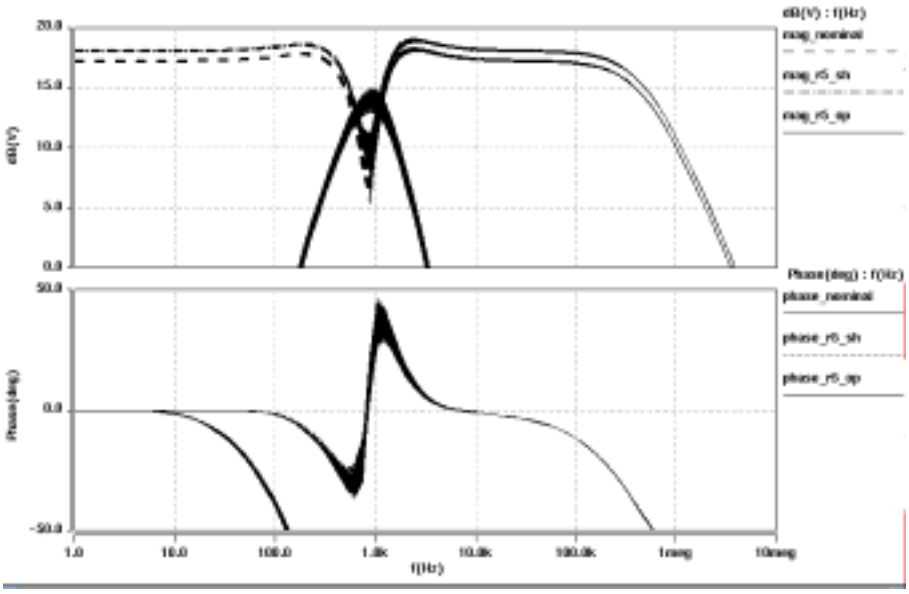

Fig. 3.2.2.2 Nominal responses, R5 open and short responses

As is shown, the frequency responses for the nominal case and R5 short/open faults were plotted. The dotted line represents R5 short fault, which is close to the nominal case. The R5 open fault differs from the nominal case significantly. Test frequencies, 100Hz, 300Hz, 500Hz, 700Hz, 800Hz, 900Hz, 1kHz, 1.5kHz, 2kHz, and 3kHz, were selected. The voltage levels at the output at each frequency were selected as features for MD measures. The MDs were calculated according to equation (3.2.1) through equation (3.2.3). In this case, only the MD between nominal and other fault cases were calculated. The calculated MD for the nominal case is from 0 to 0.3, while the MD for the R5 short fault is from 7.2 to 10.3. Clearly, a short in R5 can be detected. If the MDs were calculated against each other, the MDs between measured responses from the actual test equipment and each case should be compared to each other by using the "winner-takes-all" rule so that the faults are diagnosed. The MD between the nominal case and other cases are shown in TABLE 3.2.2.1, where op means open and sh means short.

Table 3.2.2.1 Mahalanobis Distance for Example 3.2.2.1

	mean	var	min	max
nominal	0.05	0.035	0	.28
C1=1nF	1.2meg	81.4k	1.0meg	1.3meg
C1=100nF	108.2k	1.03k	82.8k	138.7k
C2=1nF	15.1meg	1.8meg	11.9meg	18.8meg
C2=100nF	7.6k	0.7k	6.3k	9.6k
C3=1nF	19.6k	0.95k	17.5k	21.6k
C3=100nF	335k	42.2k	261k	444.4k
C4=1nF	16.7k	1.3k	13.6k	19.8k

C4=100nF	269.9k	18.2k	231.4k	310.6k
R1 op	775.4	98.6	572.6	1k
R1 sh	6.3meg	383.4k	5.5meg	7.2meg
R2 op	329.8	9.9	307.8	354.5
R2 sh	35meg	28.7meg	2.4meg	125.3meg
R3 op	66	9.3	46.6	92.6
R3 sh	230k	84.8k	92k	48.3k
R4 op	244.3k	76k	93.8k	467.9k
R4 sh	67	9.7	48.6	89.9
R5 op	58.8meg	6.2meg	41.7meg	71.8meg
R5 sh	9	0.66	7.2	10.3
R6 op	694.4k	33.4k	618.4k	796.9k
R6 sh	168.8	0.58	167.6	170.1
R7 op	2.5meg	146.8k	2.2meg	3.2me**g**
R7 sh	168.9	0.57	167.7	170
R8 op	26.7	4.4	19.8	43
R8 sh	359meg	16meg	314meg	391meg
R9 op	3.4meg	1.42meg	473.1k	7.8meg
R9 sh	26.7	4.3	19.4	38.2
R10 op	286.1	0.44	285	287.3
R10 sh	706meg	4.96meg	692meg	717meg
R11 op	8.96	0.6	7.6	10.4
R11 sh	60.8meg	6.5meg	46meg	77meg
R12 op	80.9meg	1.6meg	77.7meg	84.5meg
R12 sh	289.6	0.4	288.8	290.5

Table 3.2.2.1 can be used as the criterion for measuring whether a fault can be detected, diagnosed or be left undetected. For example, R12 short is uniquely diagnosed, while R8 open and R9 short can not be distinguished each other, but both of them are detectable.

As is seen, the MD measure in the frequency domain is very effective. However test frequencies should be chosen by some other methodologies. To avoid frequency selection, the time domain signal is sampled at discrete time steps and the sampled time series are used for generating AR models so that MD measures of AR parameters are used as criteria for analog fault diagnosis.

3.2.3 The time domain test and Mahalanobis distance

Traditionally, time domain testers were very expensive and therefore they were rarely used. However, with the wide application of DSP technology, time domain testing becomes very attractive. From the sampled time series, frequency characteristics can also be estimated, if the sampling rate exceeds the Nyquist Criterion. The sampled discrete time sequences can be easily transformed into frequency domain information by Fast Fourier Transformation (FFT). The related techniques are called spectrum estimation. If FFT coefficients are used directly in MD, the dimensionality of the covariance matrices are too large which make the evaluation process very expensive. One way of reducing the dimensionality is to find the real bandwidth of the signal. Other ways are to use spectrum estimation techniques such as the autoregressive (AR), the moving average (MA), and the autoregressive-moving average (ARMA) models. By using these models, only a limited number of the filter coefficients are used, so that dimensionality of equation 3.2.1 is greatly reduced. Figure 3.2.3.1 shows such an algorithm.

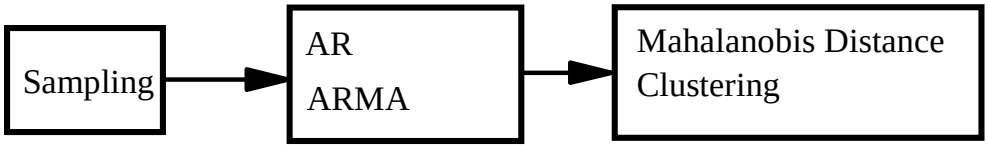

Fig.3.2.3.1(a) Simulation-before-test algorithms

Fig.3.2.3.1(b) Simulation-after-test algorithms

The three spectrum estimation models are well-known as AR, MA, and ARMA models. Many discrete-time random processes encountered in practice are well approximated by a time series or rational transfer function model [KAY88]. A driving sequence u[n] and the output sequence x[n] that are used to model the test data are related by a ARMA model and the linear difference equations,

$$x[n] = -\sum_{k=-1}^{p} a[k]x[n-k] + \sum_{k=0}^{q} b[k]u[n-k] \qquad (3.2.3.1)$$

The corresponding block diagram is shown in Figure 3.2.3.2.

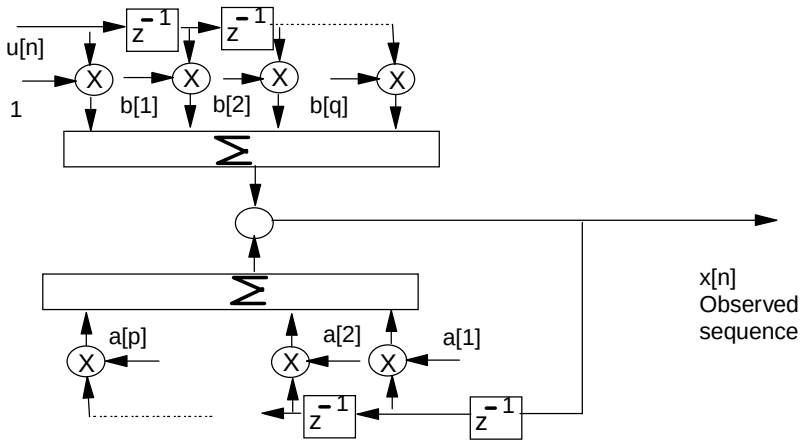

Figure 3.2.3.2 ARMA model of a random process

u[n] is an innate part of the model and gives rise to the random nature of the observed process x[n]. This model is often referred to as a pole-zero model and is denoted as an ARMA(p,q). If all the a[k] coefficients except a[0]=1 vanish from ARMA parameters,

$$x[n] = \sum_{k=0}^{q} b[k]u[n-k] \qquad (3.2.3.2)$$

and the process is strictly an MA process of order q, which is referred as an all-zero model and denoted as an MA(q) process. If all the b[k] coefficients except b[0]=1 are zero in ARMA(p,q), then

$$x[n] = -\sum_{k=-1}^{p} a[k]x[n-k] \qquad (3.2.3.3)$$

and the process is strictly an AR process of the order p, which is referred as an all-pole model and is denoted as an AR(p) process.

AR spectral estimator is the most popular approach in time series modeling. This is because accurate estimates of the AR parameters can be found by solving a set of linear equations. For accurate estimation of ARMA or MA parameters, highly nonlinear equations need to be solved. MA spectral estimation is valuable when the power spectrum density (PSD) is characterized by broad peaks. When the AR modeling assumption is valid, spectral estimations are obtained which are less biased and have a lower variability than conventional Fourier based spectral estimation. The choice of the model depends on the power spectrum density function.

The next important thing is to choose the order of the model. The best choice of the AR model order is usually not known a priori, it is necessary in practice to postulate several model orders. Model orders are selected based on some error criterion. Details of model selection methods can be found in [KAY88].

With the order of the statistical model selected we can simulate the fault-free circuit responses. Monte Carlo runs can be exploited to exercise component or process tolerances.

For each run, the parameters of the statistical model are found. Each parameter can be considered as one feature in the MD. Different runs can be used to explore various statistical properties. A cluster of the transformed measurements of the nominal circuit with tolerances parameters will be defined in the feature space. In the simulation after test stage, a measured waveform is transformed according to the chosen statistical model and the MD is found for fault detection.

Fault isolation requires that clustering will be performed for a number of Monte Carlo runs for each faulty case. MD will be then used to determine which element is at fault. However, fault isolation requires much more effort than fault detection in developing a dictionary of clusters.

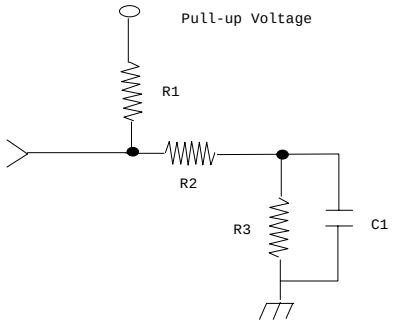

Figure 3.2.3.3 A part of an input circuitry from Figure 3.1.1.2

Example 3.2.3.1 An RC input circuitry used in automotive modules is chosen in the simulation. The circuit diagram is shown in Figure 3.2.3.3. Using Figure 3.2.3.3, an RC circuitry at a microprocessor input pin can be simulated, where R1=2KΩ, R2=27KΩ, R3=20KΩ , C1=10nF. In the simulation a step voltage signal is applied and the current through the input pin is measured. This way, instead of measuring the input impedance, a

time domain measurement is made to estimate its frequency characteristics. The measured waveform is sampled every 14.5us, so there are 1024 sample points in each simulated measurement. The real sample interval and the number of samples have to be optimized according to the actual tester and the circuit under test. In order to consider the manufacturing process, the components are randomly picked with a 5% tolerance for the resistors and a 10% for the capacitor. Normal distribution is used for all the components. Faults were simulated by changing the resistors by 50%, and making the capacitor 10 times smaller or 10 times larger than the nominal value. The test results can be generated using a circuit simulator (Saber). The 4^{th} order AR parameters are extracted using Matlab. The coefficients of AR models are used as MD features. First the nominal cases are simulated. For each feature, its mean is evaluated. For the nominal population, its covariance matrix is determined. In this case, the simulated example only considered the fault detection. The MD is found for all nominal and faulty cases. According to the histogram of MD, a fault detection threshold is determined. In this case, the threshold is found to be 11. Table 3.2.3.1 shows the simulation results.

Table 3.2.3.1 Mahalanobis distance for Example 3.2.3.1

Circuit structure	Mean	Standard Deviation
Nominal	3.81	3.063
R1 changes -50%	3184	3000
R1 changes +50%	206	70
R2 changes -50%	3177	2455
R2 changes +50%	146	156

R3 changes -50%	4.8	3.389
R3 changes +50%	8	6.566
C1 changes to 100nF	5.4*10+09	9.2*10+08
C1 changes to 1nF	4.689*10+07	1.577*10+07

In the simulation-after-test procedure, the MD for each measurement is found to determine whether it is faulty. Any MD greater than 12 can be considered as faulty. As can be seen from Table 2.4.3.1, R3 changes of 50% can not be tested. In the case where R3 changes by +50%, there could be some confusion, when compared to the case of R3 falling at -50%, as the two cases are almost identical. The poor coverage for R3 50% fault is caused by the low sensitivity of output pin characteristics v.s. R3. But if we change our target to 100% change, the fault could be better tested. In the fault diagnosis procedure, the same procedure for the nominal case has to be applied to every fault case to construct a fault dictionary.

MD and its application are discussed in this section. In the frequency domain approach, the test point selection was mentioned but not discussed. In the following section, an entropy based approach is proposed for efficient test point selection.

Example 3.2.3.2 An bandpass filter shown in Fig.3.2.3.4 is simulated. A unit step signal is applied at input terminal of the bandpass filter and the step response at output in time domain is observed. The signal is sampled every 2 microsecond for 257 sampled in total. First the 6^{th} order AR parameters are calculated according to the sampled sequences. Then, the Mahalanobis distance of these parameters are calculated.

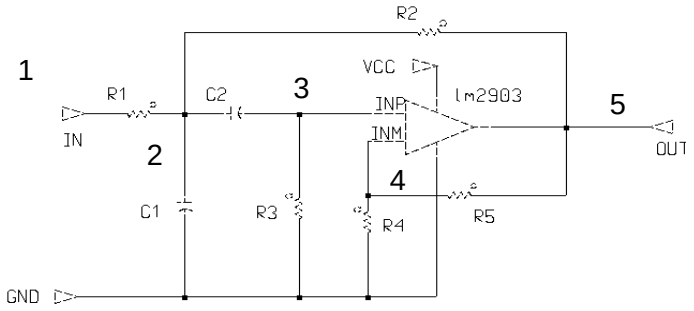

Figure 3.2.3.4 A bandpass filter

The circuit under test has been proved not diagnosable by measuring every node [DAI90] and this will be proven again in the next chapter. However fault detection is possible. In order to reduce the simulation needed, the sensitivities of the delay vs. each component are calculated and they are shown in the following table.

Table 3.2.3.2 Sensitivity matrix for bandpass filter

Component	Nominal value p_i	Sensitivity S^F_{pi}	Target $\Delta p_i/p_i$	$\Delta F/F$
R3	2k	0.803	50%	0.401
R5	4k	0.775	50%	0.3875
C1	5nF	0.611	50%	0.3
R4	4k	-0.547	50%	-0.2735
R2	1k	-0.181	50%	-0.0905
C2	5nF	-0.117	50%	-0.0585
R1	5.18k	0.096	50%	0.048

Obviously, R1 is less sensitive. Therefore, only the fault cases like R1 changes +50% and -50% are calculated in the simulation. To prove the effectiveness of AR model, Figure 3.2.3.5 shows the step response obtained by direct calculation and by the 6^{th} order AR model.

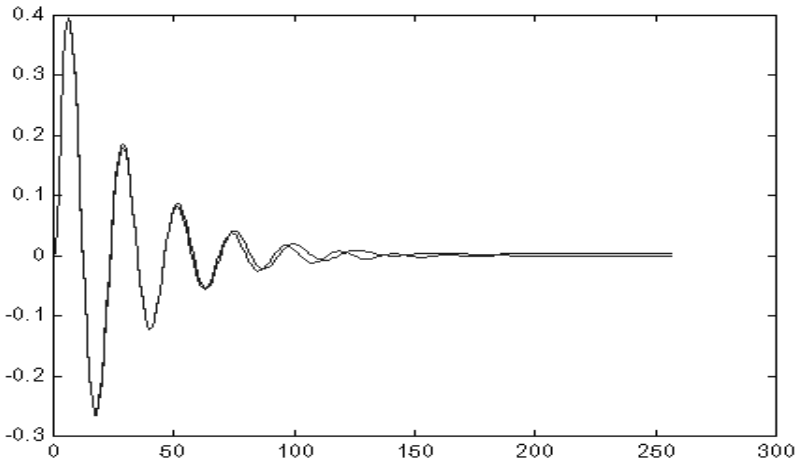

Figure 3.2.3.5 Comparison between step response and AR model

As is shown, AR model provides a good approximation of the step response of the circuit with only 6 parameters. This effectively reduces the dimension of the mahalanobis distance measure. Figure 2.3.3.6 shows the histogram representation of Mahalanobis distance of 200 Monte Carlo runs with nominal and two fault cases mentioned above, where fault1 represents R1 increase 50% fault and fault2 represents R1 decrease 50% fault. As a result, the threshold of MD can be set to 20, i.e any value in MD greater than 20 is faulty.

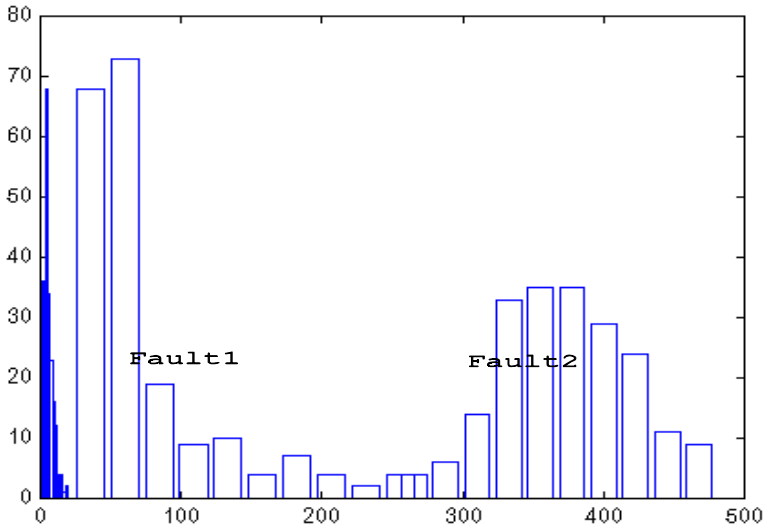

Figure 3.2.3.6 Histogram of Mahalanobis distance

In this section, ARMA model especially AR models and their applications in time domain simulation are used to reduce the dimensionality of the MD measures. The proposed AR models can be effectively used in fault simulations. In the next chapter, the selection of test points is discussed, which can be used to select the test frequencies in MD measures.

3.3 An entropy based approach for test point selection

The SBT methods are characterized by a minimum on-line computation with quite often a significant off-line computation needed to develop its database. Combinations of the fault dictionary, the probabilistic methods and the pattern recognition techniques can help us improve the fault dictionary approaches.

A fault dictionary database is a collection of potentially faulty and fault-free (nominal) measurements of a network usually simulated and organized ahead of time. The measurements could be taken at different test nodes, test frequencies, and sampling times. All of them are referred to as the test points. To describe faults in the fault dictionary, the types of stimuli (DC, AC, and time domain) and their characteristics, frequencies, and excitation levels have to be optimized. According to the simulation results, selection of the measurements is performed. The number of measurements must be kept low to reduce the testing cost, however, a maximum fault isolation should be achieved.

After the required simulation of various fault occurrences is completed, the measurements need to be selected to isolate the faults and the redundant measurements need to be eliminated. However, the candidate test points are often much larger than the number of test points which are either necessary or economically feasible to make measurements. Not all test points are equally useful. In an effort to reduce test points, Stenbakken and Souders [STE87] proposed an efficient algorithm to select test points using QR factorization of circuit sensitivity matrix. Abderrahman et al [ADB96][ADB97] used sequential quadratic programming and constraint logic programming to generate test sets. Hochward and Bastian

[HOC79], Lin and Elcherif [LIN85], Prasad and Pinjala [PRA95] used node voltages as measurements to isolate faults. Hochward and Bastian constructed ambiguity sets and applied two rules to select the test nodes. These two rules are:

- Any ambiguity set with a single fault within it uniquely defines that fault at that test node.
- Ambiguity sets whose intersection or symmetric difference results in a single fault also

  uniquely define the fault.

Lin and Elcherif [LIN85] suggested two heuristic procedures to select the test nodes using the rules of Hochward and Bastian with the computational complexity of $O(F^2N^2)$ and $O(F^2N)$ respectively, where F is the number of faults and N is the number of test nodes. The above method can not guarantee that there are no redundant test nodes. Prasad and Pinjala [PRA95] proposed a method that does not contain redundant nodes. However, the worst case time complexity of this method is exponential. Babu [BAB97] proposed three strategies for inclusive approach and three strategies for exclusive approach that improved computational efficiency of the test node selection. In this section, fault-wise table is first related to rough set theory in 3.3.1. Then, the inclusive and the exclusive approaches are discussed in 3.3.2. New entropy based approach for the test point selection is proposed in 3.3.3. It is compared with the previously developed methods. The efficiency of the proposed method is analyzed and demonstrated by an example in 3.3.4 and by computer simulation in 3.3.5.

3.3.1 Fault-wise table

For a given network, voltages or currents can be measured or simulated at the accessible test nodes to determine the network characteristics. Suppose that the voltage of a given network is analyzed for the nominal case as well as for a set of faulty conditions. At any given node, various faults may give rise to voltage values which are very close to each other, and hence it may not be possible to clearly identify the specific faulty conditions. These faults are said to be in the same ambiguity set associated with a particular node as proposed by Hochward and Bastian [HOC79]. An ambiguity set contains a list of faults which fall in a distinguished band of voltage levels, which could be determined by Monte Carlo simulation considering component tolerances, tester errors, and the optimum partition methods. Babu [BAB97] considered test point selection for the dictionary approach based on the so-called fault-wise table originally introduced in [LIN85].

In a fault-wise table, rows represent different faults (including the nominal case) and columns show the available test points. Based on the simulation results, ambiguity groups are identified and all faults which belong to the same ambiguity group of a given test point are represented by the same integer number. Since each test point represent an independent measurement, ambiguity groups of each test point are independent and can be numbered using the same integers without confusion. This way the integer coded fault-wise table is generated**.** Each column of the fault-wise table contains integers from 1 to m_n , where m_n is the number of ambiguity groups of a single test point n. In what following, the fault-wise table is defined in terms of set theory. By using the notation of set theory, we find that the

fault-wise table is a special case of the decision table developed in the rough sets theory [PAW91]. As a result, all the simplification algorithms developed for the decision tables can be applied to the fault-wise table.

Let $F=\{f_0, f_1, ..., f_k\}$ be the subset of all faults $\mathscr{F}$ and $N=\{n_1,n_2,...,n_p\}$ be the subset of all test points $\mathbb{N}$. F contains all the faults to be diagnosed on a particular fault list and N contains all the available test points, which depend on the test methodology. We associate the elements of the fault-wise table A measurement equivalent classes as follows: $\forall f_i \in F$ and $n_j \in N$, $\exists \phi (f_i, n_j) = a_{ij} \in A$ where a_{ij} is a element of the fault-wise table corresponding to the i^{th} fault and j^{th} test point. Now let $A_j=\{a_{kj} \in A\} \subset T$ be the subset of A associated with test point n_j. If for every pair (a_{mj},a_{nj}) where $a_{mj} \in A_j$ and $a_{nj} \in A_j$ $(m \neq n)$, we have $a_{mj} \neq a_{nj}$, then the system is diagnosable by test point n_j. A system is seldom diagnosable by a single testing point. When, for some $m \neq n$, $a_{mj}=a_{nj}$, then the corresponding faults f_m and f_n belong to an ambiguity set associated with test point n_j. So, if integer codes are assigned to different ambiguity sets, an ambiguity set associated with the test point n_j can be defined as $F_i^j=\{f_m \in F \mid a_{jm}=i\}$.

A fault set F can be partitioned into ambiguity sets F_0^j, F_1^j, ..., F_{k0}^j for each node n_j. Obviously for different test points, there may be different partitions of the fault set. In order to reduce ambiguity, a test point n_i is added to the previously selected nodes so that a new partition is reached. The new partition could include $F_{0,0}^{ij}$, $F_{0,1}^{ij}$, ...$F_{0,k0}^{ij}$, $F_{1,0}^{ij}$, $F_{1,1}^{ij}$, ..., $F_{1,k1}^{ij}$,..., $F_{k0,0}^{ij}$, $F_{k0,1}^{ij}$, ..., $F_{k0,kn}^{ij}$, where $F_{0,0}^{ij}$, $F_{0,1}^{ij}$, ...$F_{0,k0}^{ij} \subset F_0^i$, $F_{1,0}^{ij}$, $F_{1,1}^{ij}$, ..., $F_{1,k2}^{ij} \subset F_1^i$, ..., $F_{k0,0}^{ij}$, $F_{k0,1}^{ij}$, ..., $F_{k0,kn}^{ij} \subset F_{k0}^i$. Each new partition is based on the previous partitions. In the following, an example will be used to explain those set symbols. Table I shows a fault-wise

table with F={f_0, f_1, ...,f_8} and N={n_1,n_2, ...,n_5}.

Table 3.3.1.1 A fault-wise table

	n_1	n_2	n_3	n_4	n_5
f_0	1	1	1	0	0
f_1	0	2	0	0	0
f_2	0	0	0	2	1
f_3	0	0	0	2	0
f_4	3	0	0	3	2
f_5	2	2	0	1	2
f_6	1	2	0	4	2
f_7	3	1	1	4	1
f_8	2	0	0	1	0

Elements of the table are different equivalence classes like: $a_{01} = \phi(f_0, n_1)=1$, $a_{33} = \phi(f_3, n_3)=0$, $a_{74} = \phi(f_7, n_4)=4$. Using the test node n_1, F is partitioned into $F_0^1=\{f_1, f_2, f_3\}$, $F_1^1=\{f_0, f_6\}$, $F_2^1=\{f_5, f_8\}$, $F_3^1=\{f_4, f_7\}$. Now the second test point n_2 is added to further partition each ambiguity set. So, for the set of test points $\{n_1,n_2\}$, F is partitioned again into $F_{00}^{12}=\{f_2, f_3\}$, $F_{02}^{12}=\{f_1\}$, $F_{11}^{12}=\{f_0\}$, $F_{12}^{12}=\{f_6\}$, $F_{20}^{12}=\{f_8\}$, $F_{22}^{12}=\{f_5\}$, $F_{30}^{12}=\{f_4\}$, $F_{31}^{12}=\{f_7\}$. As we can see adding a test point reduced the uncertainty about the ambiguity sets. But this is not always true. For example, by further adding test points n_3 or n_4, the partition remains the same. If n_5 is added, the only uncertainty $\{f_2, f_3\}$ associated with test points $\{n_1,n_2\}$ can be removed. It is interesting to notice that n_5 has some special features. However, if n_5 is deleted from the test set, then $\{f_2, f_3\}$ can not be diagnosed. In order to develop test point selection for a system diagnosis, it is necessary to define diagnosability.

Definition 3.3.1 An analog system is *diagnosable* for a set of test points N_i, iff for each $i \neq j$, $\exists\, k \in N_i$ such that $a_{ik} \neq a_{jk}$.

Let us define diagnosable family $\mathbb{N} = \{ N_i \subset N \mid$ analog system is diagnosable for $N_i \}$. Then, the task of optimum test point selection is to find the $N_{min} \subset \mathbb{N}$ such that cardinality (N_{min}) is minimum, i.e. the minimum number of test points for which the system is diagnosable. Unfortunately, this problem is not polynomially bounded. So, the purpose is to have an efficient test point selection to find a local minimum set N_i for which the system remains diagnosable.

The similarity between a fault-wise table and decision table in rough set theory [PAW91] is straightforward. In a rough set, a decision table is a 3-tuple T(U,C,D) used as a knowledge representation system, in which two subsets C, D $\subset$ A of attributes are called *condition* and *decision* attributes. The decision attributes correspond to faults and condition attributes correspond to test points. In fault-wise tables, the faults have to be uniquely separated so that the decision attributes are essentially integer coded equivalence classes $D=(01...n)^T$ and are implicit in the fault-wise table. So, a fault-wise table is a special case of a decision table with one column matrix D in which no two numbers are the same. The simplification of the decision tables is equivalent to the computation of reducts and cores [PAW91]. In the following section, some simplification methods are discussed and major factors, which affect the efficiency of the algorithms, are presented in order to develop the entropy-based approach.

3.3.2. Inclusive and exclusive approaches

The fault-wise table provides information about the ambiguity set for each test point and the mutual information between test points. In view of analog fault diagnosis, the purpose is to separate the faults with a minimum number of test points. In view of the integer-coded table, the purpose is to distinguish rows based on the column information. There is no guarantee that a solution to separate all faults is available. Some heuristic methods were proposed to solve the problem [HOC79][LIN85][PRA96] [BAB97][PAW91] [ZIR93].

There are two basic approaches at the core of these methods - the inclusive and the exclusive approaches. The strategy for the inclusive approach is to add a new test point to the selected set of test points and evaluate if the separation of faults increased. The strategy for the exclusive approach is to exclude a test point, if it is not essential for the test. A test point is essential, if its exclusion degrades our separation ability. This corresponds to the concept of core in rough set theory. In the inclusive methods, redundant test points could be included in the selected test nodes. Since new test points are added sequentially, a test point may become redundant after new test points are added. In the exclusive methods, all redundant nodes are removed, but exclusive methods require longer calculation time than the inclusive methods. In view of rough set theory, inclusive methods produce discerns and exclusive methods produce reducts as defined in [STA98].

There are several heuristic strategies for selecting a measure to include a node in the inclusive methods. One measure is to select a test point which has a maximum number of ambiguity sets. Because the larger the number of ambiguity sets, the greater the probability of the faults being in the separate sets. This approach was developed and two procedures for reduction of the number of test nodes were proposed in [LIN85].

Another intuitive measure is to examine the spread of faults in the ambiguity sets. The motivation for this is to select a test point in which faults are spread uniformly across ambiguity groups. The uniform spread strategy was developed by [BAB97] and tested on a number of fault-wise tables. This algorithm has O(F*logF*N) complexity and selects the maximum spread test point at each step of the algorithm. None of these methods give the minimum number of test points needed to isolate faults.

There are also several heuristic measure strategies for the exclusive methods. Opposite to the inclusive algorithms, a test point with a minimum number of ambiguity sets may be selected for exclusion. Another measure is to exclude a test point with the highest spread of faults over the ambiguity sets. This method was also implemented by Babu [BAB97] and is analyzed in the computer simulation section in order to compare it with inclusive methods, the proposed approach, and exhaustive search approach based on rough set theory. All these test point selection techniques are closely related to the techniques of finding reducts in the rough set theory used in data mining [PAW91][ZIA94]. The new entropy based measure proposed is based on maximum information about fault separability at each step of test point selection and produces results superior to other methods discussed in the literature, as will be demonstrated through statistical analysis based on computer simulation.

3.3.3 Entropy Based Approach

In the previous section, certain heuristic measures associated with the inclusive and exclusive methods were indicated as the criterion for the test point selection. Using these heuristic measures various test point selection algorithms were developed with a main

objective to properly represent the set of faults in the fault dictionary and to solve the test point selection problem in a reasonable time. As mentioned above, the optimum test point selection is not polynomially bounded and a sub-optimal solution is the main objective of the proposed algorithm.

Hartmann et al. [HAR82] proposed a method to construct efficient decision trees by using entropy. Although the method only deals with attributes of boolean logic, it can be extended to data bases of integer or real numbers. In our approach we will discuss an entropy based approach, which deals with integer value attributes. The proposed algorithm estimates the probabilities in accordance with the cardinality of each ambiguity set. Let us assume that F_{ij} (i=1,2,...k) is the number of elements in the ambiguity set S_i for test point n_j. The probability of occurrence of an element chosen from ambiguity set S_i is approximated by F_{ij}/F. So the entropy based measure for any chosen test point n_j is expressed by

$$\begin{aligned} I_j &= -[\frac{F_{1j}}{F}\log(\frac{F_{1j}}{F}) + \frac{F_{2j}}{F}\log(\frac{F_{2j}}{F}) + \ldots + \frac{F_{kj}}{F}\log(\frac{F_{kj}}{F})] \\ &= \log(F) - \frac{1}{F}\sum_{i=1}^{k} F_{ij}\log(F_{ij}) \end{aligned} \qquad (3.3.3.1)$$

Since, in a given fault dictionary problem the number of selected faults F is fixed, the information content for the selected test point n_j in (3.3.3.1) is maximized upon minimization of the following entropy index

$$E(j) = \sum_{i=1}^{k} F_{ij}\log(F_{ij}) \qquad (3.3.3.2)$$

A test node n_j which minimizes (3.3.3.2) guarantees the largest decrease of entropy

(increase of information) by any single measurement added to the set of measurements which were previously selected. Selecting the best test node in any stage of the test selection algorithm can be easily done by a linear search for $\min_j \{E(j)\}$. Hence, the entropy based measure is an appropriate candidate for test nodes selection strategy. Accordingly, the following algorithm is proposed:

Entropy based test point selection algorithm

i. Calculate the number of elements in each ambiguity set for each test point n_j.

ii. Calculate the entropy index E(j).

iii. Add node with the minimum E(j) to the set of selected test points.

iv. Partition the fault-wise table according to the ambiguity sets for the selected set of test points.

v. If the E(j) is zero for all j or if the new E(j) is the same as the previous E(j) for all j, then stop. Otherwise, repeat (ii) - (iv).

Comments:

(1) P ambiguity sets of a chosen test point, create P partitions of the fault-wise table.

(2) If there is only one row in a partition, the corresponding fault is uniquely identified by performing measurements at the selected set of test points.

We like to point out that step (iii) guarantees a maximum information increase about the given fault diagnosis problem with selection of each new test point. Even though there

is no guarantee that the combination of these test points provide the maximum information, we reach a local information increase maximum at each stage of the algorithm. Global minimum can only be reached by an exhaustive search for a minimum set of points which minimizes system entropy. This corresponds to finding a minimum reduct in the information system [PAW91]. It was demonstrated in [SKO91] that finding a minimum reduct is NP hard, therefore there is no polynomially bounded algorithm which finds the minimum test set.

Efficiency of the proposed test point selection algorithm is high, since sorting is performed on smaller and smaller ambiguity sets. A fault table with F rows and N columns is effectively replaced by k smaller fault tables with F_1, F_2, ..., F_k rows in each table and N-1 columns. So when the sorting algorithm is applied in step (iv), it has $O(F_1\log(F_1)+...F_k\log(F_k))$ complexity, where

$$\sum_{i=1}^{k} F_i \leq F \qquad (3.3.3.3)$$

The proposed algorithm falls into the category of inclusive algorithms with a properly selected measure to optimize its performance. It has the best reported efficiency of all inclusive algorithms and yields a near optimum solution. Although numerical efficiency of the algorithm can be easily established and compared with other reported methods, its near optimality is much more difficult to prove. It is based on analysis of many statistically generated fault-wise tables and comparison with results of other algorithms including the exhaustive search which provides the optimum solution at almost exponentially increasing cost.

3.3.4 Test point selection example

In order to illustrate the entropy based test point selection, let us consider the active filter shown in Fig. 3.2.2.1. Nominal parameter values are indicated on the circuit diagram. In this example 17 catastrophic faults are considered together with the nominal case to formulate the fault dictionary

Table 3.3.4.1 Test Node measurements of an active filter circuit (Vin=1kHz, 4V)

[BAB97]

Fault class	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}
f_0 (NOM)	3.92	2.78	2.78	4.33	2.88	2.58	2.58	4.01	3.6	3.6	4.1
f_1(R1open)	8mV	6m V	6m V	9m V	6m V	5m V	5m V	8m V	3.6	3.6	7.3
f_2(R1short)	4.00	2.83	2.83	4.41	2.94	2.60	2.60	4.00	3.6	3.6	3.6
f_3(R2short)	2.84	4m V	4m V	7m V	4m V	4m V	4m V	6m V	3.6	3.6	7.3
f_4(R2short)	3.66	3.66	3.66	5.70	3.80	3.40	3.40	5.20	3.6	3.6	4.6
f_5(R3open)	2.83	2.01	2.01	2.01	1.34	1.20	1.20	1.80	3.6	3.6	5.7
f_6(R4open)	9mV	6m V	4m V	4.04	2.69	2.40	2.40	3.70	3.6	3.6	11
f_7(R5open)	3.92	2.78	2.78	4.33	3.40	3.00	3.00	4.70	3.6	3.6	5.1
f_8(R5short)	3.92	2.78	2.78	4.33	0.00	0.00	0.00	0.00	3.6	3.6	7.3
f_9(R6open)	3.92	2.78	2.78	4.33	3.87	3.80	3.87	6.00	3.6	3.6	7.3
f_{10}(R6short)	3.92	2.78	2.78	4.33	2.10	0.00	0.00	0.00	3.6	3.6	7.3
f_{11}(R7open)	3.92	2.78	2.78	4.33	2.88	2.50	2.50	2.50	3.6	3.6	5.1
f_{12}(R7short)	3.92	2.78	2.78	4.33	2.67	2.20	4m V	12.0	5.8	3.6	12
f_{13}(R8open)	3.92	2.78	2.78	4.33	2.78	2.20	1.50	12.0	5.1	3.6	12
f_{14}(R9open)	3.92	2.78	2.78	4.33	2.78	2.50	2.50	4.00	3.6	3.6	3.6
f_{15}(R9short)	3.92	2.78	2.78	4.33	2.78	2.50	2.50	4.00	4.0	3.6	12

f_{16}(R10open)	3.92	2.78	2.78	4.33	2.78	2.50	2.50	4.00	4.5	3.6	12
f_{17}(R11open)	3.92	2.78	2.78	4.33	2.78	2.50	2.50	4.00	4.0	4.0	4.7
f_{18}(R12open)	3.92	2.78	2.78	4.33	2.88	2.58	2.58	4.0	0	0	4.0

In order to obtain test measurements, a sine wave with 4 volts amplitude and 1 kHz frequency was applied to the input of the active filter circuit and the voltages were measured at nodes V_1 through V_{11}. Test point selection is performed to find the minimum number of tests (from voltage measurements at nodes 1 through 11) such that the analog system is diagnosable.

Table 3.3.4.1 lists Saber simulation results for different faulty cases. Using Table 3.3.4.1, the ambiguity sets of each test point can be found. For example, f_0, f_8 through f_{18} form an ambiguity set for the measurement at node V_1, because such a measurement can not distinguish these faulty conditions. In rough set theory this is called indiscernibility. For each ambiguity set of each test point, a different integer number is assigned to represent the set. In this example, $\{f_1, f_6\}$, $\{f_3, f_5\}$, $\{f_4\}$, and $\{f_0, f_2, f_8, f_9,..., f_{18}\}$ form four different ambiguity sets at node V_1 and are represented by the corresponding integer values 0,1,2,3 respectively. A fault-wise table is formed by assigning integer numbers to a matrix in which the ith row corresponds to the ith fault and the jth column corresponds to the jth test point. In each column of the fault-wise table identical integer numbers represent the same ambiguity set. However, identical integer numbers in different columns may represent

different ambiguity sets. Table 3.3.4.2 shows the corresponding fault-wise table for the active filter circuit.

Table 3.3.4.2 Integer coded fault-wise table for an active filter circuit

Fault	n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	n_9	n_{10}	n_{11}
f_0	3	2	2	3	3	3	4	4	1	1	1
f_1	0	0	0	0	0	0	0	0	1	1	7
f_2	3	2	2	3	4	3	4	4	1	1	0
f_3	1	0	0	0	0	0	0	0	1	1	7
f_4	2	3	3	4	6	5	6	6	1	1	2
f_5	1	1	1	1	1	1	1	1	1	1	5
f_6	0	0	0	2	3	2	3	3	1	1	8
f_7	3	2	2	3	5	4	5	5	1	1	4
f_8	3	2	2	3	0	0	0	0	1	1	7
f_9	3	2	2	3	6	6	7	7	1	1	6
f_{10}	3	2	2	3	2	0	0	0	1	1	7
f_{11}	3	2	2	3	3	3	4	2	1	1	4
f_{12}	3	2	2	3	3	2	0	8	5	1	8
f_{13}	3	2	2	3	3	2	2	8	4	1	8
f_{14}	3	2	2	3	3	3	4	4	1	1	0
f_{15}	3	2	2	3	3	3	4	4	2	1	8
f_{16}	3	2	2	3	3	3	4	4	3	1	8
f_{17}	3	2	2	3	3	3	4	4	2	2	3
f_{18}	3	2	2	3	3	3	4	4	0	0	1

According to test point selection algorithm, cardinality of each ambiguity set is established and the entropy index of each test each node is calculated yielding the following values:

Test node	n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	n_9	n_{10}	**n_{11}**
Entropy index E(j)	17.2	17.4	17.4	17.2	12.0	11.0	10.7	8.92	15.0	20.9	**6.6**

and we find that n_{11} has the minimum E(j). So n_{11} is the first node included in the set of test points. After n_{11} is chosen, the fault-wise table is partitioned into 9 sub-tables according to the ambiguity groups of n_{11}. The rearranged fault-wise table is shown in Table 3.3.4.3.

Table 3.3.4.3 Re-arranged fault-wise table after choosing n_{11}

Fault	n_{11}	n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	n_9	n_{10}
f_2	0	3	2	2	3	4	3	4	4	1	0
f_{14}	0	3	2	2	3	3	3	4	4	1	0
f_0	1	3	2	2	3	3	3	4	4	1	1
f_{18}	1	3	2	2	3	3	3	4	4	0	1
f_4	2	2	3	3	4	6	5	6	6	1	2
f_{17}	3	3	2	2	3	3	3	4	4	2	3
f_7	4	3	2	2	3	5	4	5	5	1	4
f_{11}	4	3	2	2	3	3	3	4	2	1	4
f_5	5	1	1	1	1	1	1	1	1	1	5
f_9	6	3	2	2	3	6	6	7	7	1	6
f_1	7	0	0	0	0	0	0	0	0	1	7
f_3	7	1	0	0	0	0	0	0	0	1	7
f_8	7	3	2	2	3	0	0	0	0	1	7
f_{10}	7	3	2	2	3	2	0	0	0	1	7

From Table 3.3.4.3 we see that the faults $\{f_4, f_5, f_9, f_{17}\}$ are all uniquely isolated by measuring n_{11}. We remove the corresponding rows and perform the logsum calculation on the partitioned matrix, which yields the following values for the entropy index at the indicated test nodes:

Test node	n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	**n_9**	n_{10}
Entropy index E(j)	4.81	5.42	5.42	5.42	5.53	5.65	4.21	4.82	**3.61**	7.71

with n_9 having a minimum entropy index. The remaining fault-wise matrix is then partitioned according to ambiguity sets of n_{11} and n_9 acting together. The partitioned matrix is as follows:

Table 3.3.4.4 Re-arranged fault-wise table after choosing n_{11} and n_9

Fault	n_{11}	n_9	n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	n_9	n_{10}
f_2	0	1	3	2	2	3	4	3	4	4	1	1
f_{14}	0	1	3	2	2	3	3	3	4	4	1	1
f_0	1	1	3	2	2	3	3	3	4	4	1	1
f_{18}	1	0	3	2	2	3	3	3	4	4	0	0
f_7	4	1	3	2	2	3	5	4	5	5	1	1
f_{11}	4	1	3	2	2	3	3	3	4	2	1	1
f_1	7	1	0	0	0	0	0	0	0	0	1	1
f_3	7	1	1	0	0	0	0	0	0	0	1	1
f_8	7	1	3	2	2	3	0	0	0	0	1	1
f_{10}	7	1	3	2	2	3	2	0	0	0	1	1
f_6	8	1	0	0	0	2	3	2	3	3	1	1
f_{12}	8	5	3	2	2	3	3	2	0	8	5	1
f_{13}	8	4	3	2	2	3	3	2	2	8	4	1
f_{15}	8	2	3	2	2	3	3	3	4	4	2	1
f_{16}	8	3	3	2	2	3	3	3	4	4	3	1

We can see that after selecting n_{11} and n_9 additional faults $\{f_0, f_{18}, f_6, f_{12}, f_{13}, f_{15}, f_{16}\}$ can be uniquely identified. The remaining work is performed on yet smaller tables. The procedure continues and yields the entropy measures and nodes selected as listed in Table 3.3.4.5

Table 3.3.4.5 Entropy calculated and node selected

	n_1	n_2	n_3	n_4	n_5	n_6	n_7	n_8	n_9	n_{10}	n_{11}
n_{11}	17.25	17.48	17.48	17.25	12.03	11.06	10.71	8.93	15.08	20.92	**6.62**
n_9	4.81	5.42	5.42	5.42	5.53	5.65	4.21	4.82	**3.61**	7.71	-
n_5	1.80	2.40	2.40	2.40	**1.43**	3.01	3.01	3.01	-	3.61	-
n_1	**0**	0.60	0.60	0.60	-	0.60	0.60	0.60	-	0.60	-

In Table 3.3.4.5, the bold numbers represent the minimum entropy measure. On the left, the selected nodes with the minimum entropy measure are listed. The final selection $\{n_{11}, n_9, n_5, n_1\}$ has entropy measure equal to zero, which means that these four test points can separate all faults. The corresponding program was written in MATLAB and is linked to the Saber program for generation of the fault-wise table.

For comparison, the same fault-wise table was analyzed using inclusive and exclusive strategies presented in [BAB97]. By using the inclusive strategy, a set of nodes $\{n_{11},n_8,n_7,n_5,n_9,n_1\}$ is found. Among these nodes, n_7, n_8 are redundant nodes - they can be eliminated without affecting system testability. Although Babu's inclusive algorithm is slightly slower than the proposed one, it produces significantly larger sets of test nodes. The exclusive strategy finds in this example the minimum test set $\{n_1,n_5,n_9,n_{11}\}$ which is the same as determined by the proposed entropy based approach, however, the calculation time of the exclusive algorithm is much higher. In addition, as it will be discussed in the next

section, the minimum size test sets are found less frequently using the exclusive approach than using the proposed method.

Note, that in the example circuit discussed we assumed that all the nodes are accessible for measurements, which is certainly not a practical assumption. We used it only for illustration of the test point selection process. In practice, the only requirement for this method to produce a minimum set of test points is to begin with a testable design. If the initial selection of test points described a partially testable design, then the fault-wise table contains ambiguity groups. The proposed method will then select a minimum subset from this initial set of test points, which does not degrade the circuit testability. This means that using the selected set of test points the number of ambiguity groups and their complexity remains the same as in the initial set of test points.

3.3.5 Minimum Test Sets

As it was discussed in Section IV minimum test sets can only be established through exhaustive searches and are computationally very costly. Any computationally efficient test point selection procedure must yield a suboptimum test set. It is not to say that a particular run will not reach an optimum set - it can. However, no computationally efficient procedure can be established which is guaranteed to find an optimum set in each fault dictionary. Since no theoretical proof can be given to demonstrate the optimality (except for exhaustive search methods) for a particular method, a chosen test point selection method must be tested statistically on large number of fault dictionaries in order to demonstrate its efficiency and qualities of generated test sets.

With this objective in mind several test point selection strategies were written in MATLAB and simulated on a randomly generated fault-wise tables. In the conducted statistical experiment 200 fault-wise tables were analyzed using the exhaustive search program REDUCT which generates all reducts of a given information system [STA98]. Each table had 100 simulated faults, 30 test points, and 5 ambiguity sets per each test point. Using REDUCT program minimum reducts, which correspond to minimum sets of test points were found for each fault-wise table. The same tables were analyzed using the proposed algorithm as well as using two other inclusive methods and one exclusive method and the results are compared in Table 3.3.5.1.

Table 3.3.5.1 Minimum test sets

	Percentage of the min. set of a given size found by a specified method					
Size of the min. set found	REDUCT	proposed	exclusive	inclusive 1	inclusive 2	inclusive 3
5	100	35.5	1.5	0	.5	.5
6	0	64.5	74	16.5	30	29
7	0	0	24.5	47	49.5	50
8	0	0	0	32.5	17.5	19
9	0	0	0	4	2.5	1.5

As one can see, the proposed method found minimum size test sets in 35.5% of the simulated cases, while the next best algorithm - based on the exclusive approach found minimum size test sets only in 1.5% of the simulated cases. In addition, in 24.5% the next best algorithm found minimum size test set larger by 2 than the absolute minimum size determined by the REDUCT program, while the proposed method stayed within one extra test set from the absolute minimum. All tested inclusive methods were even worse finding only .5% of the minimum test sets with about 70% of solutions larger by 2 or more from the minimum.

Not only the proposed method was superior from the compared methods in terms of its efficiency in finding near optimum solution, it was also computationally efficient. For comparison, 200 randomly generated matrices with 100 rows, 30 columns, and 5 ambiguity groups were tested in the simulation. The average simulation time tested on a 586 PC using matlab for the proposed method was 16.4 seconds per a single fault-wise table tested, while the exclusive method took 80.9 seconds and inclusive methods 1, 2, and 3 took 20.4, 27.8, and 20 seconds, respectively.

For comparison, the REDUCT program which is capable of finding the minimum test set, has faster than polynomial time dependence on the problem size as illustrated in Fig. 3.3.5.1. It took on average 2896 seconds to find a minimum test set in the fault-wise tables used in this comparative study.

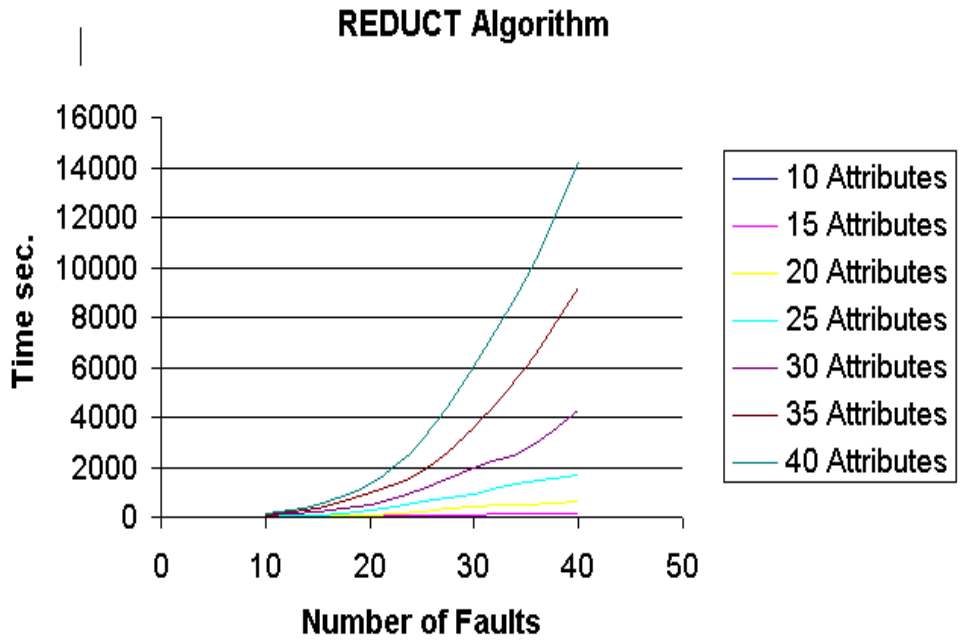

Fig. 3.3.5.1 Computational cost of the REDUCT algorithm

The number of attributes in Fig. 3.3.5.1 represents the initial size of the measurement set from which the set of test points is selected. The larger this initial set is the more costly test point selection. In addition to the time dependence on the number of faults and measurements, the algorithm's computational cost depends on the average number of ambiguity groups for each test point. Generally, the larger the number of ambiguity groups the less costly test point selection. The REDUCT program was developed and used to find the absolute minimum of the test set size in each analyzed case, but as can be seen its practical use is for small size problems only. Therefore, the importance of the proposed method is that it offers a very good quality of the selection process for large and medium size problems within a reasonable computational cost.

Chapter 4 Applications of IEEE boundary scan standards

In the previous chapter, analog testing was discussed. In this chapter, IEEE boundary scan design and its applications in mixed-signal testing are discussed. First, a brief summary of the boundary scan standards is presented in 4.1. Then, testing of analog components using the IEEE standard 1149.1 is discussed in 4.2. In order to prove the feasibility of testing analog components between boundary scan cells, the numerical algorithms for delay testing of analog fault diagnosis are studied in 4.2.1 and an analytical equation is discussed in 4.2.2. Two examples are given in 4.2.3. Finally, the proposed IEEE standard P1149.4 is discussed in 4.3.

4.1 A discussion on boundary scan standards

In this section, the discussion is divided between IEEE standard 1149.1 and the proposed IEEE standard 1149.4. A comparison is made between digital scan and analog scan by the end of this section.

4.1.1 IEEE standard 1149.1

In 1985, Philips Electronics took the lead and formed the Joint European Test Action Group (JETAG), a group of key electronics manufacturers in Europe such as British Telecom, Bull, Ericsson, Nixdorf, Siemens, and others. The aim was to reach an industry standard for PCB testing. Later in North America, companies like Texas Instrument, AT&T,

DEC and IBM joined the group and the JETAG became JTAG chaired by Philips. In 1987, the JTAG architecture version 1.0 for loaded-board testing was proposed, followed in 1988 by version 2.0. The latter version was submitted as a standard architecture to the IEEE Computer Society's Test Technology Committee. In February 1990, the document was approved by the IEEE Standards Board as IEEE Std. 1149.1-1990, and quickly achieved a great success in digital testing. Figure 4.1.1.1 Shows a standard bus architecture and Figure 4.1.1.2 shows a standard cell.

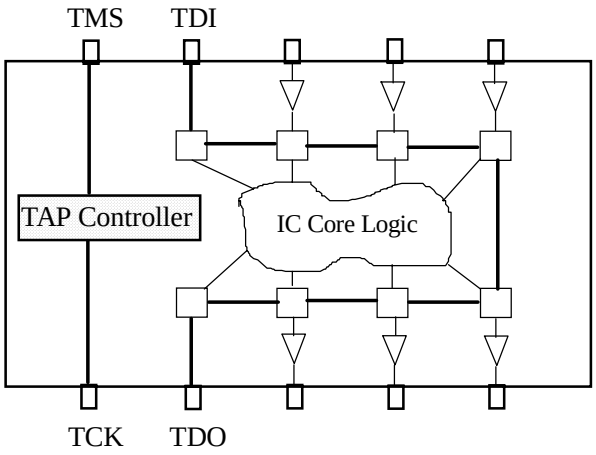

Figure 4.1.1.1 IC with TAP controller and Boundary Scan cells for digital circuit

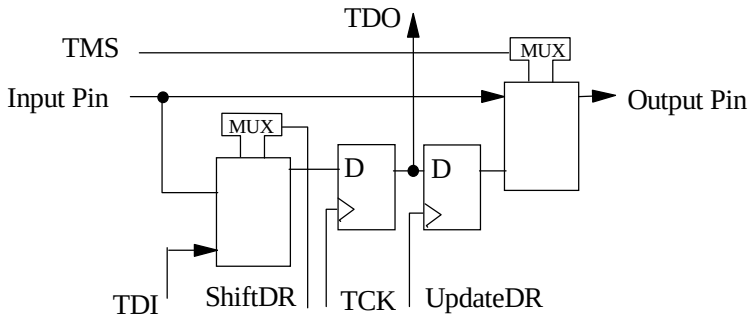

Figure 4.1.1.2 An IEEE std. 1149.1 Boundary Scan Cell

The standard provides a serial scan path through the I/O pins of ICs on a PCB board. The connectivity between components, distribution and collection of self-test or built-in-tests can be performed in a variety of series and parallel combinations. The standard includes the Test Access Port (TAP), the test architecture, the TAP controller, the Instruction Register (IR), Test-Data Register (DRs), and boundary scan registers.

The TAP is a definition of the interface that needs to be included in an IC to make it capable of being included in a Boundary-Scan architecture. The port has four or five pins described as follows: The Test Clock Input(TCK) pin is used to control test clock into and out of the chips. The Test Mode Select(TMS)pin is used to control test operation. The Test Data Input(TDI)pin is used to input series test data to a chip and the Test Data Output (TDO) pin is used to shift out series test data from a chip. The Test Reset Signal (TRST)is an optional pin used to asynchronously reset the TAP controller.

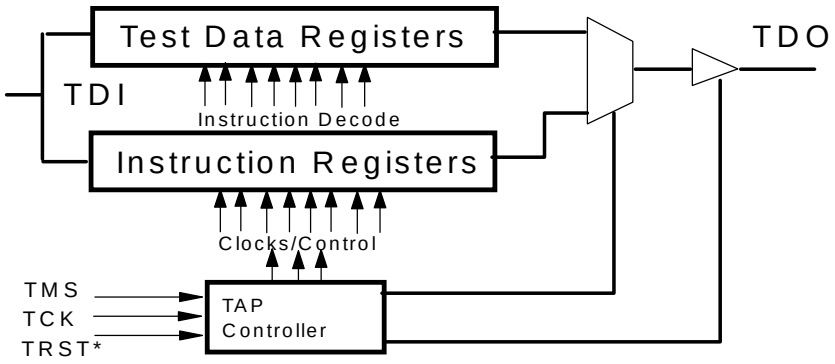

Figure 4.1.1.3 The TAP architecture

The basic test architecture that must be implemented on a chip consists of the TAP interface pins, a set of test data registers to collect data from the chip, an instruction register, and a TAP controller as shown in Figure 4.1.1.3.

The TAP controller is a 16 state FSM (Finite State Machine) that precedes from state to state based on the TCK and TMS signals. It provides signals that control the DRs and IR. The state diagram is shown in Figure 4.1.1.4. The state transition is that of TMS signal at the rising edge of TCK.

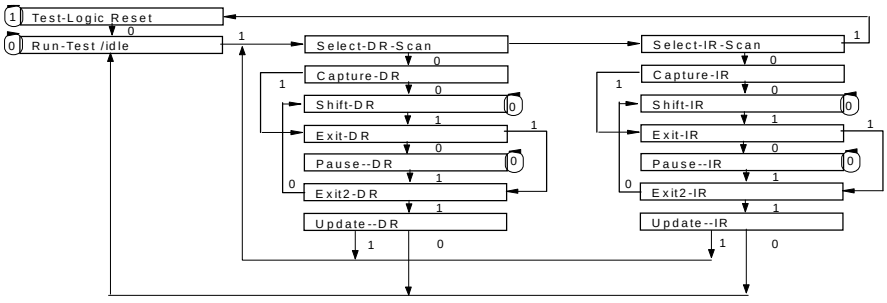

Figure 4.1.1.4 TAP controller state diagram

The IR has to be at least two bits long to decode at least three instructions described as follow: BYPASS is represented by an IR having all zeros and it is used to bypass any serial-data registers in a chip with a 1 bit register. EXTEST allows for the testing of off-chip circuitry and is represented by all ones. SAMPLE/PRELOAD places the boundary-scan registers in the DR chain and either sample or preload the chip I/Os. In addition to the tree instructions mentioned above, there are two more instructions recommended by the standard which are INTEST and RUNBIST. INTEST allows for a single-step testing of internal circuitry via the boundary scan registers. RUNBIST is used to run internal self-testing procedures within a chip. EXTEST is used to isolate the core circuitry from the boundary scan circuit and selectively drive a logic 0, logic 1, or high impedance at any output pin.

DRs are used to set the inputs of the modules to be tested, and to collect the results of running the tests. The simplest data-register configuration is a boundary-scan register passing through all I/O and a 1-bit long bypass register. Boundary Scan Register is a special case of a data register.

4.1.2 IEEE Proposal P1149.4

IEEE standard 1149.1 has achieved great success in digital PCB board testing. On the other hand, analog components such as pull-up resistors, EMC protection capacitors, and power supply circuits are still present on a pure digital PCB board. In addition, mixed signal PCB boards are used increasingly in many applications. It is necessary to investigate mixed signal testing. In an effort to extend the idea of IEEE 1149.1 to mixed signal circuit testing,

some analog testability boundary scan bus structures were proposed [PAR93][THA93][LOF96]. The proposed IEEE standard structure is based on IEEE standard 1149.1 and the implementation is shown in Figure 4.1.2.1.

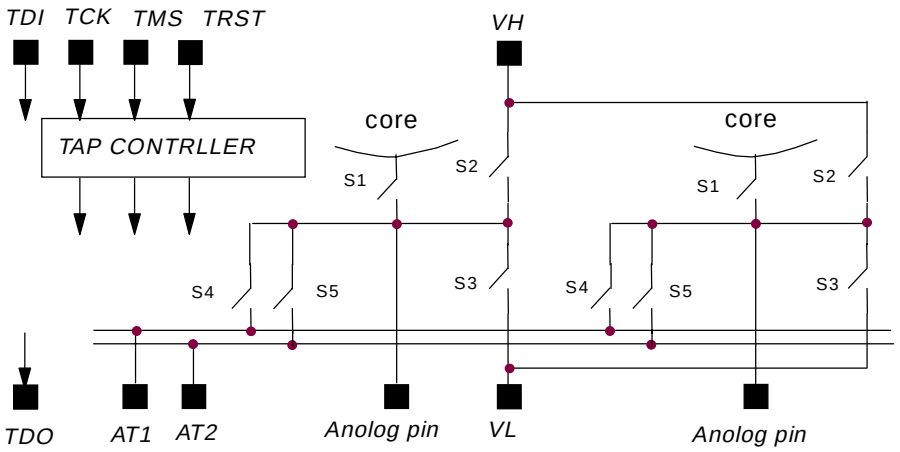

Figure 4.1.2.1 The structure for the proposed IEEE standard 1149.4

As is seen, the structure requires two analog pins in addition to the four mandated digital pins, TCK, TMS, TDI, and TDO. The structure allows for the testing of interconnect failures such as shorts and opens, the testing of discrete analog components and the network between ICs, and also supports the testing of analog functions within the ICs themselves. The structure requires two analog buses AT1 and AT2 and identical networks for each I/O pin. The networks are referred to as analog boundary scan cells or ABCs. Additional pin count is one of the major concerns for IEEE Proposed Standard P1149.4. Some researchers began to look at pin reduction. A different test structure was proposed by Lu and R. Dandapani [LU93], which requires only one analog pin in addition to the IEEE std. 1149.1 digital pins. David J. Cheek and R Dandapani [CHE94] proposed another test structure which views the

TMS pin as a mixed-signal pin and uses it for stimulus during analog measurement, and for logic input during control of TAP controller state transitions. R. Russell proposed a method for achieving mixed-signal test objectives within established 1149.1 pin/wiring overheads [RUS96], in which TMS and TCK pass both analog and digital signals. In this work, the possibility of using IEEE std. 1149.1 to test the analog interconnections will be studied using a new delay based approach. The implementation of this approach will permit savings of two pins for each chip. While using IEEE standard 1149.1 in analog testing one needs to consider the loading effect which requires a simulation before tests.

4.1.3 Analog scan v.s. digital scan

For the simple PCBs used in automotive and consumer electronics, the component verification method discussed in chapter three is effective. For a cluster of analog circuitry in a digital PCB board, the digital scan method provides a good solution. For the very expensive PCBs with a lot of analog circuitry on it, if the test resolution is very high, the test bus method compatible with the proposed standard IEEE P1149.4 may be an answer. In the system level solution for error detection in analog and mixed-signal circuits, the internal blocks of an analog circuit are accessed using virtual probes controlled by IEEE standard 1149.1.

Two basic concepts of the boundary scan approach are circuit partitioning and test signal scanning. The implementation of circuit partitioning in analog circuits is the leading topic of discussions of the Working Group for the IEEE P1149.4 mixed-signal test bus

standard. However, there are fundamental differences between analog and digital testing, which make duplication of the solutions satisfactory for digital testing difficult to adopt for analog testing. When a digital switch is inserted into the signal path of a digital circuit to enforce circuit partitioning, its effect can be tolerated. In the worst case, an extra delay is needed. In an analog circuit, insertion of a switch into the signal path may cause a major deformation of the signal itself, which must be corrected at the design stage.

Scanning is also more difficult in analog systems than in digital systems. First there is no reliable analog memory or shift register cells which can be used in high speed applications. Second, any distortion of the analog signal along the interconnection lines may have a significant effect on the test results.

An attempt to implement test signal scanning was made [WEY92], but a practical implementation of this approach is limited. The analog signal is sampled to be shifted out for evaluation. Distortion of the analog signal shifted through a chain of the registers will cause inaccuracies in the analog signal evaluation. In addition, the proposed scan chain does not have the benefit of the digital scan path.

An alternative to signal scanning is to either evaluate the tested signal at the test point locations using built in signal transformation networks and comparators, or to preprocess the analog signal locally, transform the resulting signal to a digital form, and shift it out for evaluation using boundary scan organizations for digital signals. The following is a discussion for such a scheme.

4.2 Testing of analog interconnections with std. IEEE 1149.1

Let us first consider a cluster of analog components as a filter between chips as shown in Figure 4.2.1.

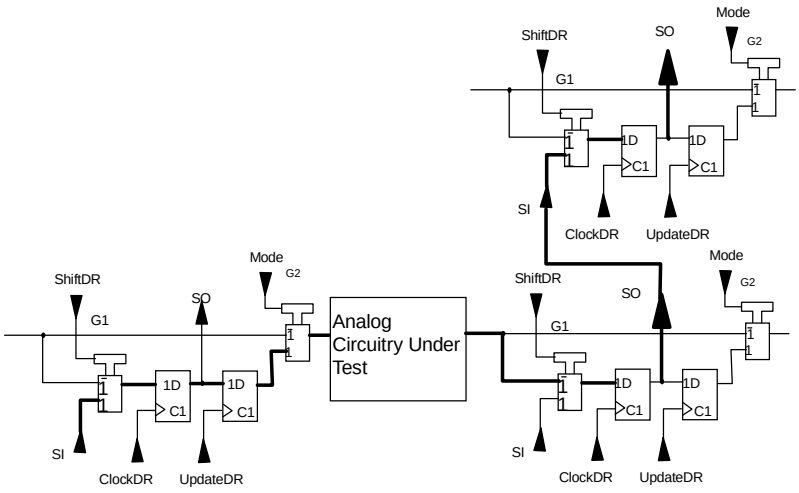

Figure 4.2.1 An analog cluster with the IEEE boundary scan cells

A pulse train is applied from the cell_1 which is connected to the input of analog circuitry under test (CUT). By observing the response at cell_2 which is connected to the output of the analog CUT , a constant 1 or 0 would be "seen", or a sequence 0101... would be "seen" depending on the time constant of the filter as well as the clock and duty cycle of the waveform applied. In order to tell the bad circuitry from the good ones, the waveforms must be properly designed. Let us look at a low pass filter network shown in Figure 4.2.2, where R1= 10kΩ.

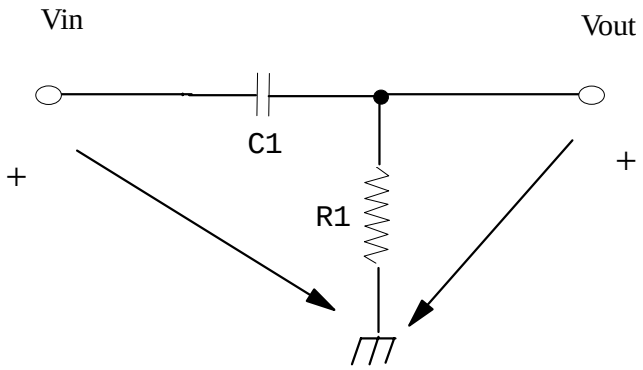

Figure 4.2.2 A high pass filter

When a waveform as shown in Figure 4.2.3 is applied to input pin and when capacitances are changed, we will see two different responses, as shown also in Figure 4.2.3.

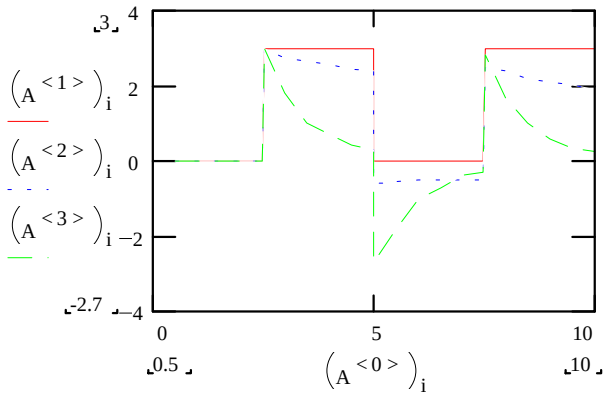

Figure 4.2.3 The input and output of the low pass filter for different capacitor values

The solid line represents a digital input signal with 5ms period. The longer dashed line represents the output voltage when C is 0.1uF and the dotted line represents the response when C is 1uF. If a level sensitive digital chip is connected to the output pin and we evaluate 1's and 0's at every 1ms, we will get two different sequences. One is 0010000100 and the

other is 0011100111. Those sequences can be shifted out through the IEEE standard 1149.1 bus for evaluation. The possibility of testing a mixed-mode signal system by using IEEE std. 1149.1 only is studied in this section. First, numerical delay equations are conducted in 4.2.1, then, analytical equations are discussed in 4.2.2. Section 4.2.1 and section 4.2.2 are essentially presented as the preparation toward the testing of analog components using digital boundary scans. In section 4.2.3, an example filter and its responses will be discussed in connection to the IEEE 1149.1 bus and control circuit.

4.2.1 Delay testing

The world is full of analog information. So, why are the digital ways of information storage and transmission is so dominating today? The answer heavily relies upon the digital form being easy to store and easy to transfer without substantial distortion. Even though sampling and digitizing analog information introduces distortion, the degree of distortion can be controlled. In addition, analog information is distorted in storage and transmission anyway. The function of boundary scan is to transmit information out for evaluation. It works just like communication. The analogy between digital communication and boundary scan can help us better understand how to transform analog information into boundary scan cells. What makes digital communication and digital signal processing (DSP) so successful is the sampling theory and quantization.

The sampling theory says that if the sampling rate is greater than or equal to two times the maximum frequency of an analog signal, the analog signal can be fully recovered

from its sampled data. Because of the sampling theory, pulse-amplitude modulation (PAM), pulse-width modulation (PWM), and pulse-position modulation were developed. PWM tells us that analog information can be carried by the pulse delays. Therefore, it is possible to evaluate the characteristics of analog signals by measuring the delays. This idea can be used in analog fault diagnosis by observing the delays of analog signals.

After an analog signal is sampled, quantization converts the sampled data into a stream of binary digits for transmission, using for instance, delta modulation (DM). So, it is possible to digitize the delay information. Later, the idea of using IEEE standard 11491.1 to digitize such delay information will be discussed. As a result, the digitized information is transmitted to the testers through boundary scan cells in the IEEE 1149.1 standard for evaluation. The advantage of transforming analog information into digital information is to minimize the distortion due to shifting of analog signals and signal interferences which result from implementation of the IEEE proposed P1149.4 standard. The question is how can the delay information be used? How to digitize analog information into boundary scan cell? And what is the limitation for such a method? In order to answer these questions, delay equations are discussed for the testability measures this section, analytical equations are discussed in next section for waveform design, and the use of IEEE 1149.1 standard is discussed section 4.2.3.

The time domain equation of a circuit is formulated [VAL94] as:

$$\begin{aligned} C\dot{\boldsymbol{x}} + G\boldsymbol{x} &= \boldsymbol{w} \\ F &= \boldsymbol{d}^{t}\boldsymbol{x} \end{aligned} \qquad (4.2.1.1)$$

where bold letters represent vectors, **x** is the voltage and current vector, **x** dot represents dx/dt vector, **G** is the resistive element matrix, **C** is the reactive element matrix, **w** is the input vector, and F is the corresponding output which is the linear combination of voltage and current **x** transformed by vector **d**. In order to calculate the delays, a threshold V_H is introduced. At a particular time t_{nom}, the analog signal should equal to V_H. Due to some fault in the circuit, the faulty analog signal can arrive at V_H at time t_{fault}. We will demonstrate how the delay $\tau = t_{nom} - t_{fault}$ can be used to decide if the CUT is faulty. Assume that

$$\begin{aligned} &F(\boldsymbol{p},t)=V_H \\ &\boldsymbol{p}=(p_1,p_2,...,p_m) \end{aligned} \qquad (4.2.1.2)$$

Where V_H is a specified threshold voltage. Equation (4.2.1.2) implies that its solutions are evaluated at some discrete time t_i. Obviously, F is the function of parameters p_i and time t_i. t_i is also the function of parameters. Taking the derivative of equation (4.2.1.2) vs. parameters, we have

$$\frac{\partial F(\boldsymbol{p},t)}{\partial p_i}+\frac{\partial F(\boldsymbol{p},t)}{\partial t}\frac{\partial t}{\partial p_i}\Big|_{F(\boldsymbol{p},t_i)=V_H}=0 \qquad (4.2.1.3)$$

So, the sensitivity of t_i vs. a parameter p_i can be expressed as

$$\frac{\partial t}{\partial p_i}\Big|_{F(\boldsymbol{p},t_i)=V_H}=-\frac{\dfrac{\partial F(\boldsymbol{p},t)}{\partial p_i}\Big|_{F(\boldsymbol{p},t_i)=V_H}}{\dfrac{\partial F(\boldsymbol{p},t)}{\partial t}} \qquad (4.2.1.4)$$

The corresponding discrete equations for equation (4.2.1.1) are formulated as

$$C\dot{\boldsymbol{x}}_{\boldsymbol{n}}+G\boldsymbol{x}_{\boldsymbol{n}}=\boldsymbol{w}_{\boldsymbol{n}}$$
$$F_n=\boldsymbol{d}^{\,t}\boldsymbol{x}_{\boldsymbol{n}} \qquad (4.2.1.5)$$

Taking the derivative of both sides of equation (4.2.1.5) vs. parameter p_i, we have

$$C\frac{\partial\dot{\boldsymbol{x}}_{\boldsymbol{n}}}{\partial p_i}+\frac{\partial C}{\partial p_i}\dot{\boldsymbol{x}}_{\boldsymbol{n}}+G\frac{\partial\boldsymbol{x}_{\boldsymbol{n}}}{\partial p_i}+\frac{\partial G}{\partial p_i}\boldsymbol{x}_{\boldsymbol{n}}=\frac{\partial\boldsymbol{w}_{\boldsymbol{n}}}{\partial p_i} \qquad (4.2.1.6)$$

Let us use new discrete time variables s_n and u_n defined as follows

$$\boldsymbol{s}_{\boldsymbol{n}}=\frac{\partial\boldsymbol{x}_{\boldsymbol{n}}}{\partial p_i}$$
$$\boldsymbol{u}_{\boldsymbol{n}}=-\frac{\partial C}{\partial p_i}\dot{\boldsymbol{x}}_{\boldsymbol{n}}-\frac{\partial G}{\partial p_i}\boldsymbol{x}_{\boldsymbol{n}}+\frac{\partial\boldsymbol{w}_{\boldsymbol{n}}}{\partial p_i} \qquad (4.2.1.7)$$

and we have

$$C\dot{\boldsymbol{s}}_{\boldsymbol{n}}+G\boldsymbol{s}_{\boldsymbol{n}}=\boldsymbol{u}_{\boldsymbol{n}} \qquad (4.2.1.8)$$

Note that (4.2.1.8) has the same form as (4.2.1.5)

Now choose one of the differential equation forms:

$$\dot{\boldsymbol{x}}_{\boldsymbol{n}}=\frac{1}{h}(\boldsymbol{x}_{\boldsymbol{n}}-\boldsymbol{x}_{\boldsymbol{n-1}})\quad n=1$$
$$\dot{\boldsymbol{x}}_{\boldsymbol{n}}=\frac{2}{h}(\boldsymbol{x}_{\boldsymbol{n}}-\boldsymbol{x}_{\boldsymbol{n-1}})-\dot{\boldsymbol{x}}_{\boldsymbol{n-1}}\quad n\geq 2 \qquad (4.2.1.9)$$
$$h=t\ -t\ ,$$

where t_1, t_2, ... t_n are discrete time steps for each iteration. Other differential equation forms could also be used. In order to formulate iteration equations for calculating a sensitivity matrix, we rewrite equation (4.2.1.5) as

$$C\dot{\boldsymbol{x}}_n + G\boldsymbol{x}_n = \boldsymbol{w}_n \qquad (4.2.1.10a)$$
$$C\dot{\boldsymbol{x}}_{n-1} + G\boldsymbol{x}_{n-1} = \boldsymbol{w}_{n-1} \qquad (4.2.1.10b)$$

together with (4.2.1.10a) and (4.2.1.10b), we have

$$C(\dot{\boldsymbol{x}}_n + \dot{\boldsymbol{x}}_{n-1}) + G(\boldsymbol{x}_n + \boldsymbol{x}_{n-1}) = \boldsymbol{w}_n + \boldsymbol{w}_{n-1} \qquad (4.2.1.11)$$

and from (4.2.1.9), we have

$$\dot{\boldsymbol{x}}_n + \dot{\boldsymbol{x}}_{n-1} = \frac{2}{h}(\boldsymbol{x}_n - \boldsymbol{x}_{n-1}) \qquad (4.2.1.12)$$

From (4.2.1.5) and (4.2.1.9) we get the equation for n=1 and combining (4.2.1.11) and (4.2.1.12), we have the following iteration equations

$$\begin{aligned} &(\frac{1}{h}C + G)\boldsymbol{x}_n = \frac{1}{h}C\boldsymbol{x}_{n-1} + \boldsymbol{w}_n \quad n = 1 \\ &(\frac{2}{h}C + G)\boldsymbol{x}_n = (\frac{2}{h}C - G)\boldsymbol{x}_{n-1} + \boldsymbol{w}_n + \boldsymbol{w}_{n-1} \quad n \geq 2 \end{aligned} \qquad (4.2.1.13)$$

Equation (4.2.1.13) is from Dai's work [DAI90]. Similarly, we can get the same form of equation for $\mathbf{s}_n$. After finding $\mathbf{s}_n$, $\mathbf{x}_n$, and $d\mathbf{x}_n/dt$, from equation (4.2.1.4) and (4.2.1.1), we can have the following equations:

$$\frac{\partial F(\boldsymbol{p},t)}{\partial p_i} = \boldsymbol{d}^{\,t}\frac{\partial \boldsymbol{x}(\boldsymbol{p},t)}{\partial p_i}$$
$$\frac{\partial F(\boldsymbol{p},t)}{\partial t} = \boldsymbol{d}^{\,t}\frac{\partial \boldsymbol{x}(\boldsymbol{p},t)}{\partial t} = \boldsymbol{d}^{\,t}\dot{\boldsymbol{x}} \qquad (4.2.1.14)$$

so that we have

$$\frac{\partial t}{\partial p_i}\Big|_{t=t_i} = -\frac{\boldsymbol{d}^{\,t}\boldsymbol{s}_n}{\boldsymbol{d}^{\,t}\dot{\boldsymbol{x}}_n} \qquad (4.2.1.15)$$

for n≥2, rewrite equation (4.2.1.15) for step n and n-1

$$\boldsymbol{d}^{\,t}\left[\frac{2}{h}(\boldsymbol{x}_n - \boldsymbol{x}_{n-1}) - \dot{\boldsymbol{x}}_{n-1}\right]\frac{\partial t}{\partial p_i}\Big|_{t=t_i} = -\boldsymbol{d}^{\,t}\boldsymbol{s}_n \quad (a)$$
$$\boldsymbol{d}^{\,t}\left[\frac{2}{h}(\boldsymbol{x}_{n-1} - \boldsymbol{x}_{n-2}) - \dot{\boldsymbol{x}}_{n-2}\right]\frac{\partial t}{\partial p_i}\Big|_{t=t_i} = -\boldsymbol{d}^{\,t}\boldsymbol{s}_{n-1} \quad (b) \qquad (4.2.1.16)$$

Add (a) and (b) in equation (4.2.1.16) and from (4.2.1.7),(4.2.1.9),(4.2.1.12), and (4.2.1.14) we have

$$\frac{\partial t}{\partial p_i}\Big|_{t=t_i} = -h\frac{\boldsymbol{d}^{\,t}\boldsymbol{s}_n}{\boldsymbol{d}^{\,t}(\boldsymbol{x}_n - \boldsymbol{x}_{n-1})} \qquad n=1$$
$$\frac{\partial t}{\partial p_i}\Big|_{t=t_i} = \frac{-h}{2}\frac{\boldsymbol{d}^{\,t}(\boldsymbol{s}_n + \boldsymbol{s}_{n-1})}{\boldsymbol{d}^{\,t}(\boldsymbol{x}_n - \boldsymbol{x}_{n-1})} \qquad n\geq 2 \qquad (4.2.1.17)$$

For n different t_i's and m parameters, we can have equations which relate time delays to changes in parameter values:

$$\sum_{j=1}^{m} S_{ip_j} \frac{\Delta p_j}{p_j} = \Delta t_i \qquad (4.2.1.18)$$

Let $\mathbf{S}_{NM}=\{S_{ipj}\}$, $\Delta\mathbf{p}/\mathbf{p}=(\Delta p_1/p_1, \Delta p_2/p_2, \ldots, \Delta p_m/p_m)$, $\Delta\mathbf{t}=(t_1,t_2,...,t_n)$. Equation (4.2.1.18) can be written in matrix form:

$$\boldsymbol{S}_{NM} \frac{\Delta \boldsymbol{p}}{\boldsymbol{p}} = \Delta \boldsymbol{t} \qquad (4.2.1.19)$$

The rank of the sensitivity matrix determines the solvability of the circuit using time delay measurements. If $\mathbf{S}_{NM}$ has the full rank, then

$$\frac{\Delta \boldsymbol{p}}{\boldsymbol{p}} = \boldsymbol{S}_{NM}^{-1} \Delta \boldsymbol{t} \qquad (4.2.1.20)$$

If the measurement error in Δt is δ, then the estimated parameter error is $\mathbf{S}_{NM}^{-1}\delta$.

For the case when the number of measurements n is greater than the number of parameters, we can solve (4.2.1.19) using pseudo inverse to obtain

$$\frac{\Delta \boldsymbol{p}}{\boldsymbol{p}} = (\boldsymbol{S}_{NM}^{t} \boldsymbol{S}_{NM})^{-1} \boldsymbol{S}_{NM}^{t} \Delta \boldsymbol{t} \qquad (4.2.1.21)$$

with the estimated parameter error determined by $(\mathbf{S}_{NM}^{t}\mathbf{S}_{NM})^{-1}\mathbf{S}_{NM}^{t}\delta$.

If the rank of matrix S_{NM} is smaller than the number of parameters, the circuit is not solvable. In this case, we should reduce the number of unknowns in the equation, i.e. some components have to be assumed nominal. If multiple faults are to be solved, the permutation

of different conditions will make the problem very difficult to solve. In most cases, a single fault is assumed.

If all the component changes are within its nominal tolerance range and if we denote ΔT the resulting Δt in equation (4.2.1.19), Then only those faults which make $S_{ipj}*(\Delta p/p)$ greater than ΔT can be detected.

Let us now study an example shown in Figure 3.2.3.4. The ranks of its sensitivity matrix $\mathbf{S}_{NM}$ for different measurement are simulated using MATLAB and the results are shown in Table 4.2.1.1

Table 4.2.1.1 Test nodes and ambiguity groups

No of test nodes	Test nodes	Rank
1	5	3
	3	3
	2	4
2	3,5	4
	2,5	5
3	2,3,5	5
4	2,3,4,5	5

It is not surprised that the conclusion is the same as Dai work [DAI90). However, the result is obtained through delay sensitivity equations instead of time measurement as was used in Dai's paper. There are 7 components and the highest rank for delay sensitivity matrix is only five, even every node is accessible. Therefore, the circuit is unsolvable by measuring

node 2 through 5. As a result, only fault detection can be considered for this circuit. In example 4.2.3.2, a fault detection case will be given for this circuit.

The presented parameter identification based on time delay requires direct measurement of time delay in analog sub-circuit. In an embedded system, this may be impossible due to inaccessability of the analog output. Therefore, in order to make this approach attractive to a modern PCB design, an equivalent information must be obtained in a digital form and scanned out for evaluation. The rationale behind delay analysis is to transform analog delay information into digital one, according to a preset threshold. That is to say that if a fault can cause significant delay, say a few gate delay, the faulty information can be carried out into digital forms. A detailed explanation as well as a analytical form will be presented next.

4.2.2 Fault diagnosis through delay analysis

We just discussed how to use numerical delay equations in analog fault diagnosis. In order to transform delay information into a digital scan cell, we now study the analytical representation of charging and discharging for a first order system. Figure 4.2.2.1 shows three analog signals with different time constants and the corresponding digital signals (shown as signals 1 through 3).

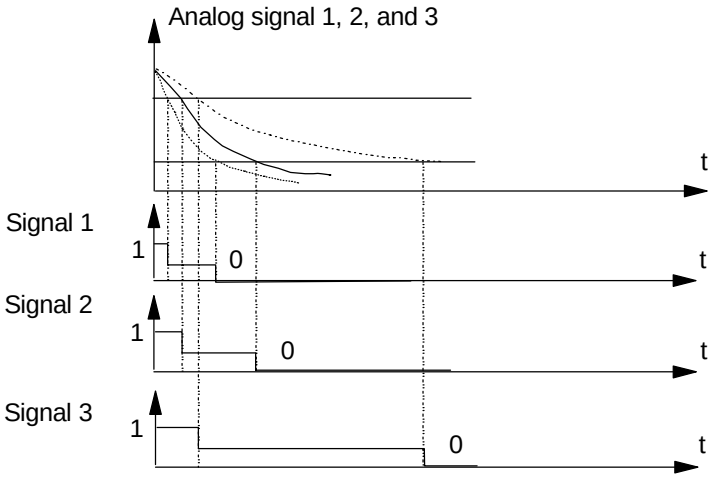

Figure 4.2.2.1 Exemplary analog signal and its digital waveforms

In order to illustrate the delay analysis, let us consider the input and output waveforms of an analog cluster as shown in Figure 4.2.2.2.

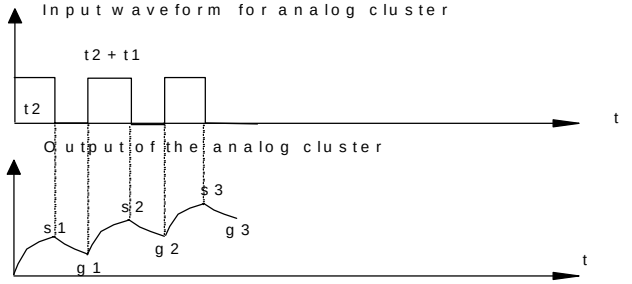

Figure 4.2.2.2 Input and output signal for an analog circuit

Between time intervals $(0,t_2)$,(t_2,t_2+t_1), $(t_2+t_1,2t_2+t_1)$, and $(2t_2+t_1,2(t_2+t_1))$, etc., the corresponding waveforms are described analytically by $s_1(t)$, $g_1(t)$, $s_2(t)$, $g_2(t)$,... and etc, where

$$
\begin{aligned}
s_1(t) &= A(1-e^{-\frac{t}{\tau_2}}) \\
s_2(t) &= A(1-e^{-\frac{t}{\tau_2}}) + g_2 e^{-\frac{t}{\tau_2}} \\
s_n(t) &= A(1-e^{-\frac{t}{\tau_2}}) + g_{n-1} e^{-\frac{t}{\tau_2}}
\end{aligned}
\qquad (4.2.2.1)
$$

and

$$
\begin{aligned}
g_1(t) &= s_1 e^{-\frac{t}{\tau_1}} \\
g_2(t) &= s_2 e^{-\frac{t}{\tau_1}} \\
&\cdots \\
g_n(t) &= s_n e^{-\frac{t}{\tau_1}}
\end{aligned}
\qquad (4.2.2.2)
$$

Where τ_2 is the rise time constant and τ_1 is the fall time constant. The extreme values of these functions at their time limits can be expressed as s_1, g_1, s_2, g_2, ..., s_n and g_n, where $s_i=s_i(t_2)$ and $g_i=g_i(t_1)$. Now let us test the convergence of sequences $\{s_n\}$ and $\{g_n\}$. Since

$$
\begin{aligned}
|s_n - s_{n-1}| &= |g_{n-1} e^{-\frac{t_1}{\tau_1}} - g_{n-2} e^{-\frac{t_1}{\tau_1}}| \\
&= |A(1-e^{-\frac{t_2}{\tau_2}}) + s_{n-1} e^{-\frac{t_2}{\tau_2}} - A(1-e^{-\frac{t_2}{\tau_2}}) - s_{n-2} e^{-\frac{t_2}{\tau_2}}| e^{-\frac{t_1}{\tau_1}} \\
&= |s_{n-1} - s_{n-2}| e^{-\frac{t_2}{\tau_2}} e^{-\frac{t_1}{\tau_1}} \le |s_{n-1} - s_{n-2}|
\end{aligned}
\qquad (4.2.2.3)
$$

Sequence $\{s_n\}$ converges. Similarly, since

$$|g_n - g_{n-1}| = |s_n - s_{n-1}| e^{-\frac{t_2}{\tau_2}} \qquad (4.2.2.4)$$

we get

$$\begin{aligned} |g_{n-1} - g_{n-2}| &= |s_{n-1} - s_{n-2}| e^{-\frac{t_2}{\tau_2}} \\ &= |s_n - s_{n-1}| e^{-\frac{t_2}{\tau_2}} e^{\frac{t_1}{\tau_1}} e^{\frac{t_2}{\tau_2}} \\ &= |s_n - s_{n-1}| e^{\frac{t_1}{\tau_1}} \\ &= |g_n - g_{n-1}| e^{\frac{t_1}{\tau_1}} e^{\frac{t_2}{\tau_2}} \geq |g_n - g_{n-1} \end{aligned} \qquad (4.2.2.5)$$

So, sequences $\{s_n\}$ and $\{g_n\}$ converge, When n approaches infinity, then $s_n \to s$ and $g_n \to g$ where the limit extreme values are expressed by

$$s = A(1 - e^{-\frac{t_2}{\tau_2}}) + ge^{-\frac{t_2}{\tau_2}} \qquad (4.2.2.6)$$

and

$$q = se^{-\frac{t_1}{\tau_1}} \qquad (4.2.2.7)$$

s and g represent the final extreme values which limit the oscillations of the analog output waveform.

$$s = \frac{A(1 - e^{-\frac{t_2}{\tau_2}})}{1 - e^{-(\frac{t_1}{\tau_1} + \frac{t_2}{\tau_2})}} \qquad (4.2.2.8)$$

$$g = \frac{A(1 - e^{-\frac{t_2}{\tau_2}})}{1 - e^{-(\frac{t_1}{\tau_1} + \frac{t_2}{\tau_2})}} e^{-\frac{t_1}{\tau_1}} \qquad (4.2.2.9)$$

By properly designing the input waveform, we should be able to get different digital sequences for a fault-free circuit and faulty circuits in which parameters change beyond specified limits. Since the signal level of the digital waveform is fixed for a given technology, the key to the waveform design is proper selection of the time interval for discharge, t_1 and the time interval for charge, t_2. Since τ_1 and τ_2 are determined by the circuit parameters, by designing t_1 and t_2 and using equations for s(t), g(t), we can generate digital sequences for both fault free and faulty circuits. Different digital sequences can be produced for different time constants. Thus characterizing different faulty cases. Equations (4.2.2.8) and (4.2..2.9) define limits for the analog signal produced by the analog filter. If a fault is present, these values will change as illustrated in Figure 4.2.2.3.

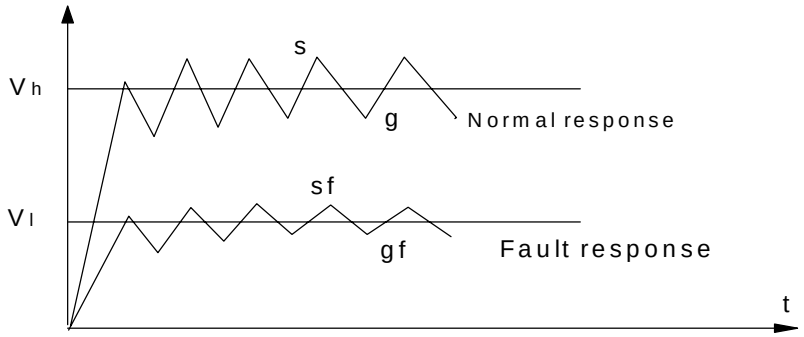

Figure 4.2.2.3 Nominal signature and fault signature

Let τ_1 and τ_2 be time constants for the normal circuit and τ_{f1} and τ_{f2} be time constants for a faulty circuit. Substituting these constants into equations (4.2.2.8) and (4.2.2.9), we get s and g for the normal circuit and s_f and g_f for a faulty circuit. We will assume that the threshold voltage for a logic 0 is lower than V_l and for a logic 1 is higher than V_h, where V_l and V_h depend on the design technology used. The voltage level between V_l and V_h will be considered as an unknown logic value. Comparing a fault-free waveform with a faulty waveform, we may have the cases summarized in Table 4.2.2.1:

TABLE 4.2.2.1 Logic values for normal and fault circuitry

	Conditions	Normal	Fault
Case 1	$g>V_h$ and $s_f<V_l$	Logic 1	Logic 0
Case II	$s<V_h$ and $g_f>V_h$	Logic 0	Logic 1
Case III	$s>V_h$ $V_h>g_f>V_l$ $V_h>S_f>V_l$ $G_f<V_l$	Oscillating between logic 1 and don't care	Oscillating between logic 0 and don't care
Case IV	$s_f>V_h$ $V_h>g_f>V_l$ $V_h>s>V_l$ $g<v_l$	Oscillating between logic 0 and don't care	Oscillating between logic 1 and don't care
Case V	$S_f>V_h$ $g_f>V_l$ $s>V_l$ $g<V_l$	Oscillating between logic 1 and logic 0	Oscillating between logic 1 and don't care

In case I and II, the nominal case and faulty case are obviously different. Therefore, the fault is detectable. In a waveform design, these two cases are the most desirable. However, it is sometimes impossible to design a waveform like what is shown in case I and

case II.

In case III, VI, and V, the transformed normal digital sequence is oscillating between logic 0 and logic 1 and the faulty sequence is also oscillating between logic 0 and logic 1. The only difference is the degree of oscillating. Hence, whether the fault is detectable or not depends on the delays. In order to detect fault, different sequences should be presented for nominal case and faulty cases. This presents problems for waveform design. In order to overcome such difficulties, a pseudo random generator like linear feedback shift register (LFSR) can be used to the input of analog circuit, because LFSR generated signal has a wide band of spectrum [AI92]. The purpose of using LFSR is to have the circuit under test exposed to different randomly generated pulse width. Therefore, waveform design and its difficulties are avoided.

In the following section, how to use boundary scan standard to shift out analog information is discussed. Two example will be given to prove the feasibility of the proposed method.

4.2.3 Testing of analog components using boundary scan

Form above discussions, digital signals can be captured and shifted out for detailed analysis using digital boundary scan cells. Parameter information contained in these digital signals can be extracted by analyzing the obtained responses.

If the applied waveform is periodic, we can observe the output waveform without strict timing control. The limitation of the method is that it can only test low frequency

components. The sampling rate and the number of sampling data depend on the analog signal frequency.

Now, we discuss the scanning of digital input and output test signals into analog clusters. A typical IEEE 1149.1 boundary scan cell has been shown in Figure 4.1.1.2 and the cell configuration on a PCB with analog cluster has been shown in Figure 4.1.1.1 in section 4.1.1. In order to shift out analog information, the standard cell should work either as a rectangular waveform generator on the analog circuit input or as a simple A/D converter on the analog output. As we can see from Figure 4.1.1.1, if we set ShiftDR in the input cell to logic 1 and set the Mode selection to 1, the input boundary scan cell in analog input circuitry could function as a signal generator. The digital sequence is generated according to the delay characteristics of analog circuit into boundary scan cell connected to analog output. On the other hand, if we set ShiftDR of boundary scan cell in the output of analog circuitry to logic 0, than we can read digital data from D latch and shift out to the next cell and later to the boundary scan path in Figure 4.1.1.1. Note that ShiftDR is usually a common pin, so we have to control the ShiftDR of each cell separately, which means added logic to standard TAP controller.

The digital data shifted out can be evaluated using pattern recognition techniques. One way of doing this is to use neural networks. After the computer simulation, the digital sequences are obtained so that the comparison can be made between the nominal and faulty cases. Due to component tolerances, we will have a class of sequences for the nominal circuit and other classes for faulty circuits.

The neural network used in this example will be Radial basis networks. It may require more neurons than standard feedforward backpropagation networks, but usually, they take just a fraction of time to train compared with the feedforward backpropogation approach. That means a reduced simulation time in simulation-before-testing. Since radial basis networks are easy to train and work best when many training vectors are available, they are selected for the neural network training in this work. Matlab based simulation of a radial basis neural network was used in the simulation example. The output is recalled by referring to the generated neural network organization and using a prepared set of test vectors. An example is given to illustrate this approach.

Example 4.2.3.1. In the example, the fault list was generated according to the discussion of section 2.3. The faulted components were changed to 0.1 and 10 times the nominal values in the simulation of the manufacturing testing. Remaining components have their values within nominal values plus or minus 3 times their standard deviation (related to design tolerances). The analog circuit was placed as shown in Figure 4.2.3.1 between two chips with boundary scan cells, where r2=(2kΩ,±5%), r3=(27kΩ,±5%), c1=(1nF,±10%), c2=(10nF, ±10%).

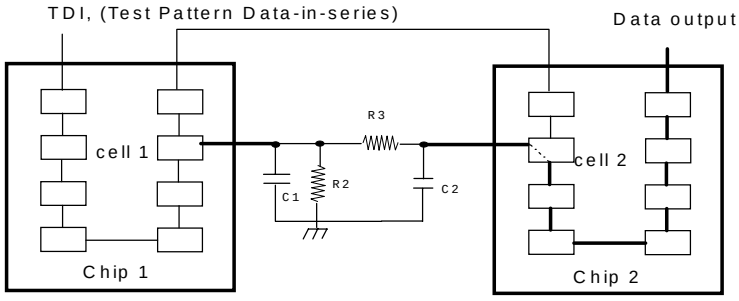

Figure 4.2.3.1 An analog filter between two chips boundary scan cells

The simulation set up is shown in Figure 4.2.3.1. Saber software simulator with Monte Carlo options is used to obtain circuit responses.

In order to have a "good" sequence for testing, a pulse train with the width of half the nominal time constant and 50% duty cycle was chosen. The digitized analog output is what we want to examine. In this method, analog signal frequency must be at least one order of magnitude less than digital clock frequency. This limits the bandwidth of analog testing using the proposed approach. From the circuit time constant, we know that for changes of C1 within 0.1 to 10 times its nominal values, we can only produce minimal time constant changes. So, we choose C1 to change from 1pF to 1uF in order to produce more significant output deviations. Actually, C1 is much more easier to test, if we reverse the analog input and output.

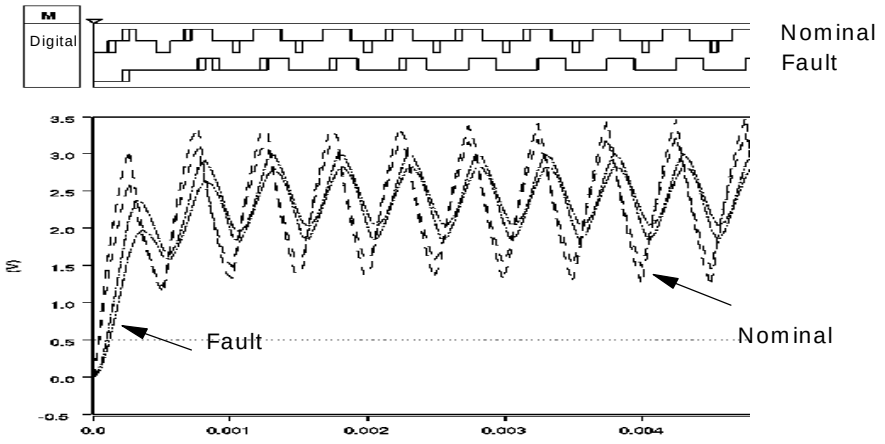

Fig. 4.2.3.2 The analog signals at analog output and their converted digital sequences

Fig.4.2.3.2 shows the difference between the nominal digital signature and a faulty

digital signature as well as their respective analog waveforms. Note, that for both conditions, 200 Monte Carlo runs were made and CMOS signal levels were used to determine the A/D conversion.

We sample the digital data from Fig.4.2.3.2 every 50u seconds to produce 100 data points for each signature. In this example vector length could be reduced to 10 without sacrificing the accuracy of the fault diagnosis. To diagnose the faults, a radial based neural network from Matlab Neural Network Toolbox is used. Data shown in Figure 4.2.3.3 were used, which represents signatures in NN training. C1 fault is undetectable, because C1 is essentially parallel with signal generator. we chose not to use C1 fault case (Note: By reversing input and output, C1 fault can be detected). In neural network training, we have one normal case and seven fault signatures.

Each signature has 200 Monte Carlo runs and each run contains 100 data points. After producing response signatures, we run a data reduction program to select independent waveforms for NN training. After using the data reduction program, we have 21 waveforms for nominal case, 8 waveforms for C1=1uF, 5 for C2=1nF, 11 for C2=100nF, 7 for R2=2.7kΩ, 15 for R2=270kΩ, 15 for R3=2kΩ, and 12 for R3=20kΩ. We choose some signatures for training of the neural network and the remaining signatures for testing. To obtain the training set, 21 signatures were selected from the nominal case, 4 from C1=1uF, 3 from C2=1nF, 6 from C2=100nF, 4 from R2=2.7kΩ, 8 from R2=2.7kΩ, 8 from R3=0.2kΩ, and 6 from R3=20kΩ. The respective test data matrix was assigned with 1 for the normal case and 2 for each of the faulty cases. After simulation we have successfully tested the neural network and detected faulty circuitry. Although the test was performed on a small set

of waveforms, it demonstrated that this approach can be used successfully for fault detection. The optimum waveform design and sample rate need to be studied further for better test vector generation and shorter test time. Fig. 4.2.3.3 shows the nominal signature and signatures of several faulty cases.

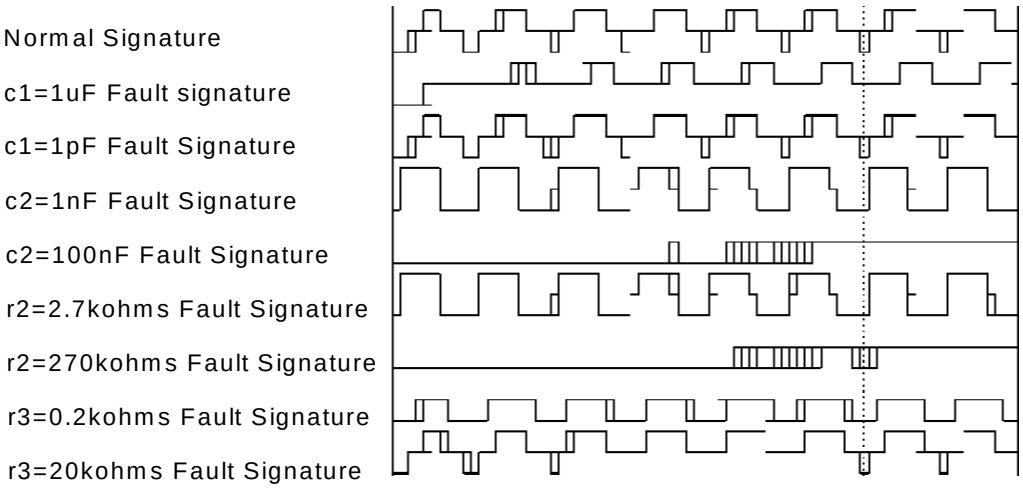

Figure 4.2.3.3 No fault signature vs. fault signatures

The above example proves that analog faults can be diagnosed by IEEE 1149.1 boundary scan cells. The waveform design is somewhat ad hoc. In order to make the fault visible, waveform design can be performed according to what was discussed in section 3.2. However, there are other methods which are far more superior, for instance, pseudo noise sequences. The advantage of such a sequence is that different waveform duty cycles can be applied to the circuit under test. The following example will explain the advantages of using pseudo random generator as input waveform generator.

Example 4.2.3.2. In this example, a pseudo random generator is used to generate the

input signal to circuit under test. The clock frequency is chosen according to the rise time and fall time, usually one half the value. Therefore, the generated pseudo random sequence will have various pulse width input to the CUT. The following block diagram shows the simulation setup.

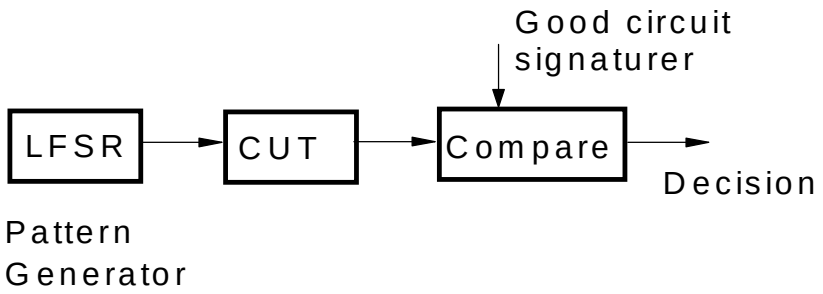

Figure 4.2.3.4 Simulation block diagram for LFSR method

Based on above setup and the filter shown in Figure 4.2.1.1 is used in CUT, the simulation was done with 200 Monte Carlo runs to simulate manufacturing. In order to reduce simulation effort, the sensitivities of delay vs. each components were calculated. Then, the component which gave the smallest change was picked for simulation. In this case, it was R1 and R1 was 5.18kΩ. The two fault cases were R1=1kΩ and R1=11kΩ. The results are shown in Figure 4.2.3.5 and Figure 4.2.3.6. Figure 4.2.3.5 shows the digital signal at input to CUT, analog signal at output of the CUT and transformed digital form of the analog signal. Figure 4.2.3.6 shows nominal signature and two faulty signatures.

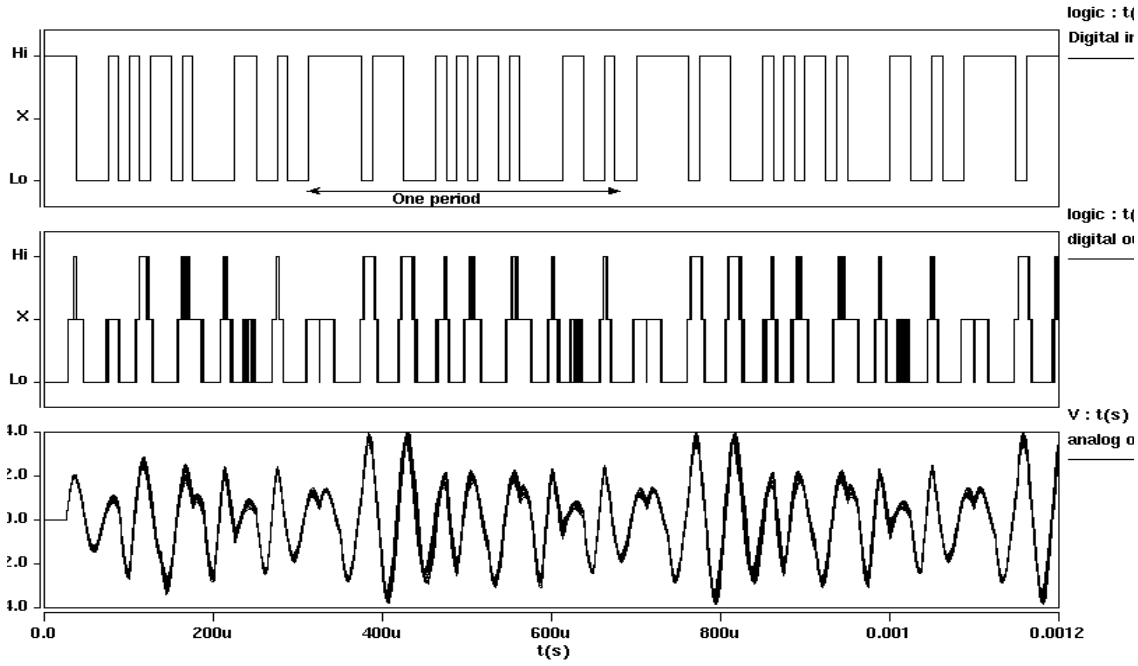

Figure 4.2.3.5 Input digital sequence and analog output at CUT and its digital form

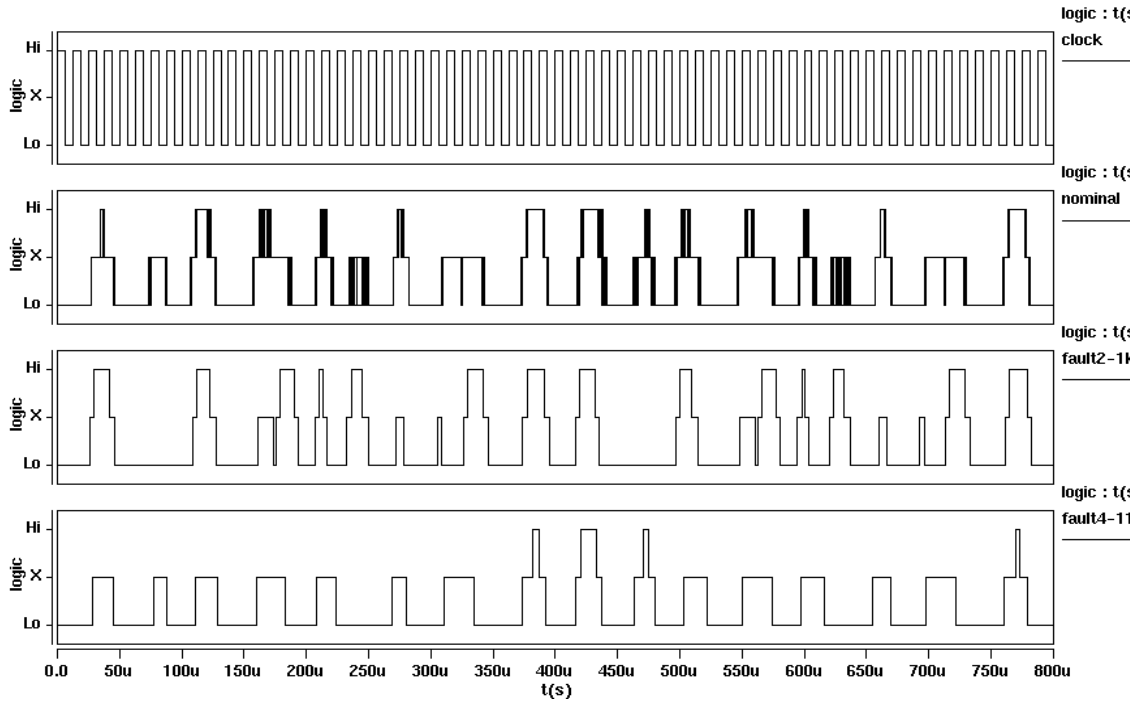

Figure 4.2.3.6 nominal signature vs. faulty signatures II

4.3 A "Virtual Probe" test bus compatible with IEEE 1149.1

In order to observe analog signal more directly, an approach to observing the analog signal values is to use analog test bus connected directly to the output of a tested circuit. Such a test bus could be connected to test points through analog switches organized in a similar way to the digital boundary scan cells. The digital boundary scan cells are used to control the connections between the node to be tested and the tester. Figure 4.3.1 shows an exemplary realization of the analog boundary scan bus (ABSB) and an analog boundary scan cell. The difference between the proposed bus and IEEE P1149.4 is that the analog switches are avoided in the signal path to reduce the signal distortion introduced by additional switches.

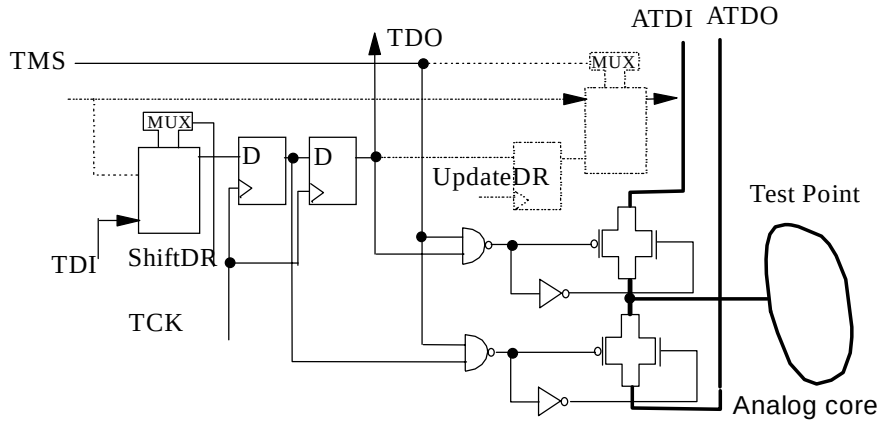

Figure 4.3.1 An analog boundary scan cell

This cell is activated in the test mode by the test mode select (TMS) signal. An analog boundary scan cell connects a selected test point (TP) to the analog bus. The analog bus contains two wires which carry analog test data input (ATDI) and analog test data output (ATDO) signals. A test point can be connected to either ATDI or ATDO line by setting a

corresponding analog switch inside the ABS cell. The switches are controlled by D-latches and activated by the TMS signal. Note that the analog switch is placed outside the normal signal path, the loading effect can be minimized by connecting a high impedance voltmeter to ATDO. If a test signal is to be injected to a test point, the ATDI bus is connected to a current source.

If differential signals are to be tested, the output signal may be connected to two different ATDO lines.

Individual ABS cells are cascaded and connected to various test points (TP) inside the analog circuit. In order to select a specific TP, its address is shifted through the sequence of D-latches inside the cascaded analog boundary scan cells along TDI and TDO lines. Not only can all the input and output pins of analog circuits be tested using this structure, but all the internal test points, critical to verify the circuit performance, can be tested as well. During the sequential shift operation, test points are disconnected from analog bus. Chip level organization of the analog test bus with its ABSB cells is shown in Figure 4.3.2.

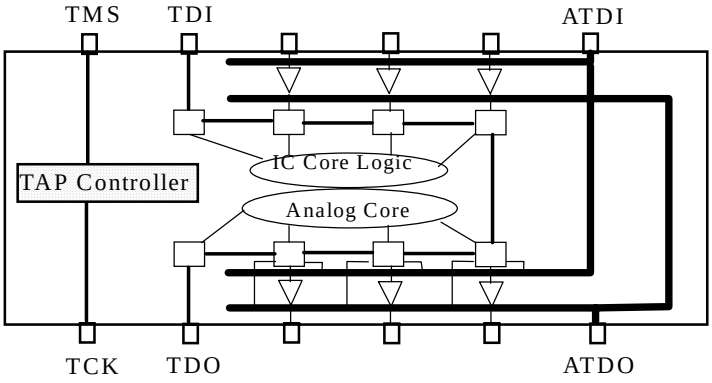

Figure 4.3.2 An IC level boundary scan with TAP controller

This structure can be then extended to the board and system levels, in which all chips

are scanned sequentially in a fashion similar to digital boundary scan. In order to demonstrate the feasibility of such analog test bus, Motorola ANSWB100, a 100-ohm body-effect analog switch cell with single enable and 176X128 grids, was used as analog switch in simulation. The analog switch symbol and its equivalent circuit is shown in Figure 4.3.3

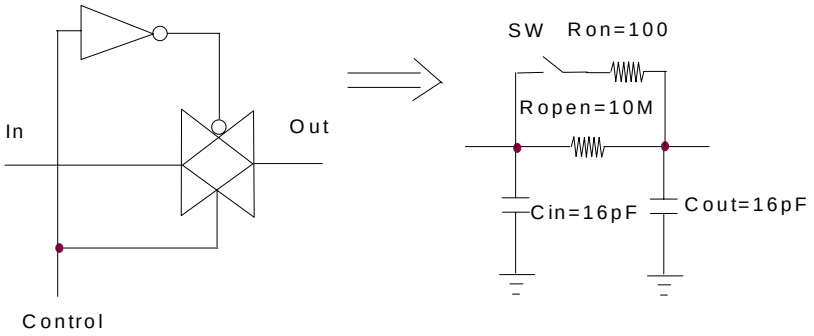

Figure 4.3.3 Analog switch symbol and its equivalent circuit

The system level equivalent circuit for IEEE standard P1149.4 and the proposed ABSB are shown in Figure 4.3.4 and 4.3.5 respectively.

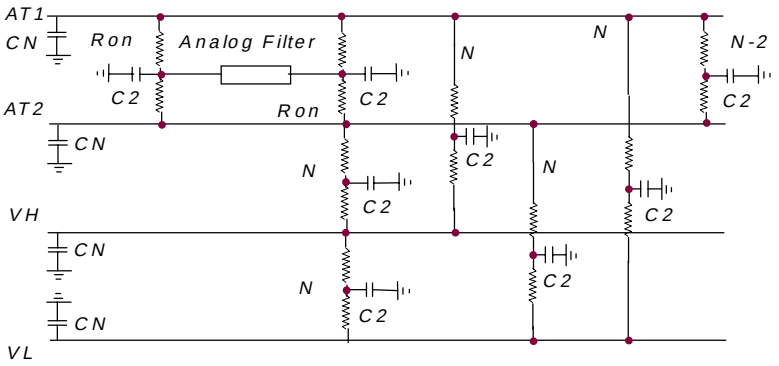

Figure 4.3.4 The equivalent circuit for IEEE P1149.4

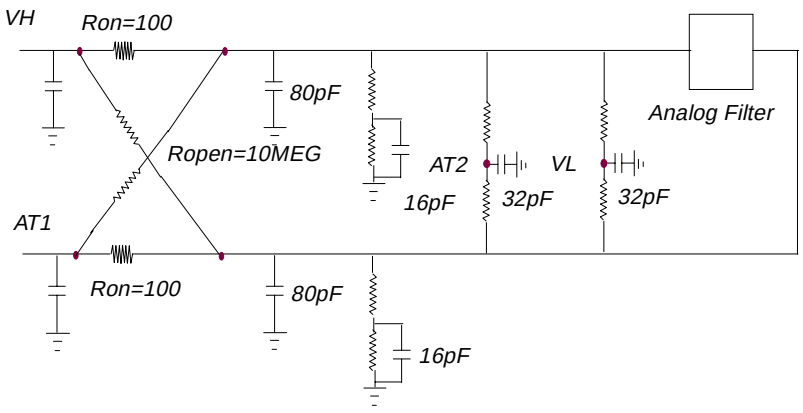

Figure 4.3.5 The equivalent circuit for proposed ABSB

First, the analog boundary scan bus consists of 22 cells and a filter circuit connected between ATDI and ATDO was simulated. A step signal is applied to ATDI and the simulated output signal at ATDO is shown in Figure 4.3.6. In the same plot, the direct step response of the filter is also shown the same figure. Therefore, it is feasible to used analog boundary scan cell to virtually probe analog nodes inside the chip or PCB board if the loading and frequency effects are not significant.

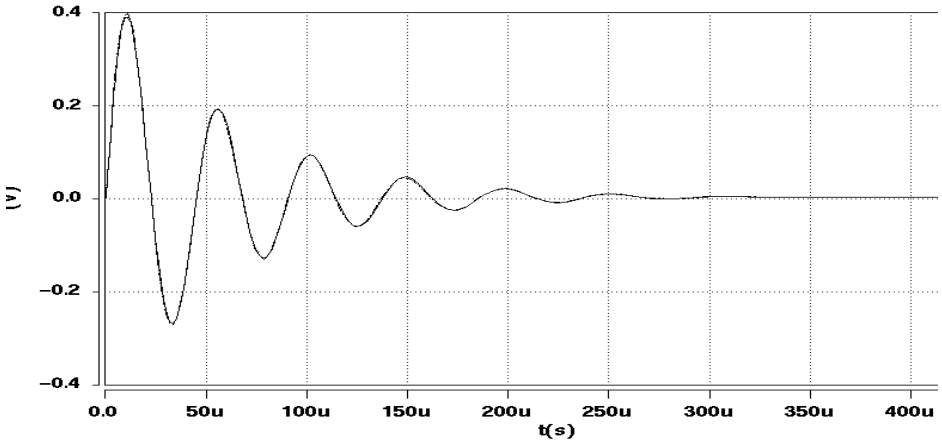

Figure 4.3.6 Step response at analog bus AT2 vs. direct output

Even though analog boundary scan cells can be used, its limitation must be aware of. In the following, IEEE P1149.4 and proposed ABSB are compared each other. Different number of boundary scan cells, for instance, 22 cells and 8 cells, are also compared. Figure 4.3.7 and 4.3.8 show the Z-parameters of analog bus. In these two figures, only z_{11} and z_{12} are shown, because of its symmetry.

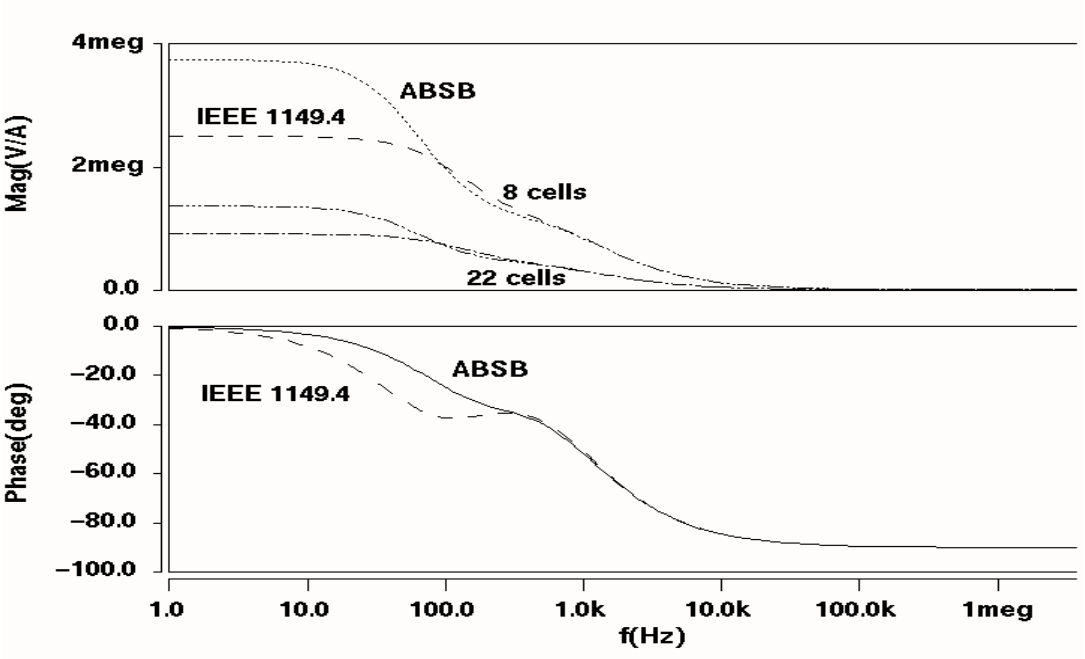

Figure 4.3.7 z_{11} parameters for IEEE 1149.4 and ABSB with 8 and 22 cells

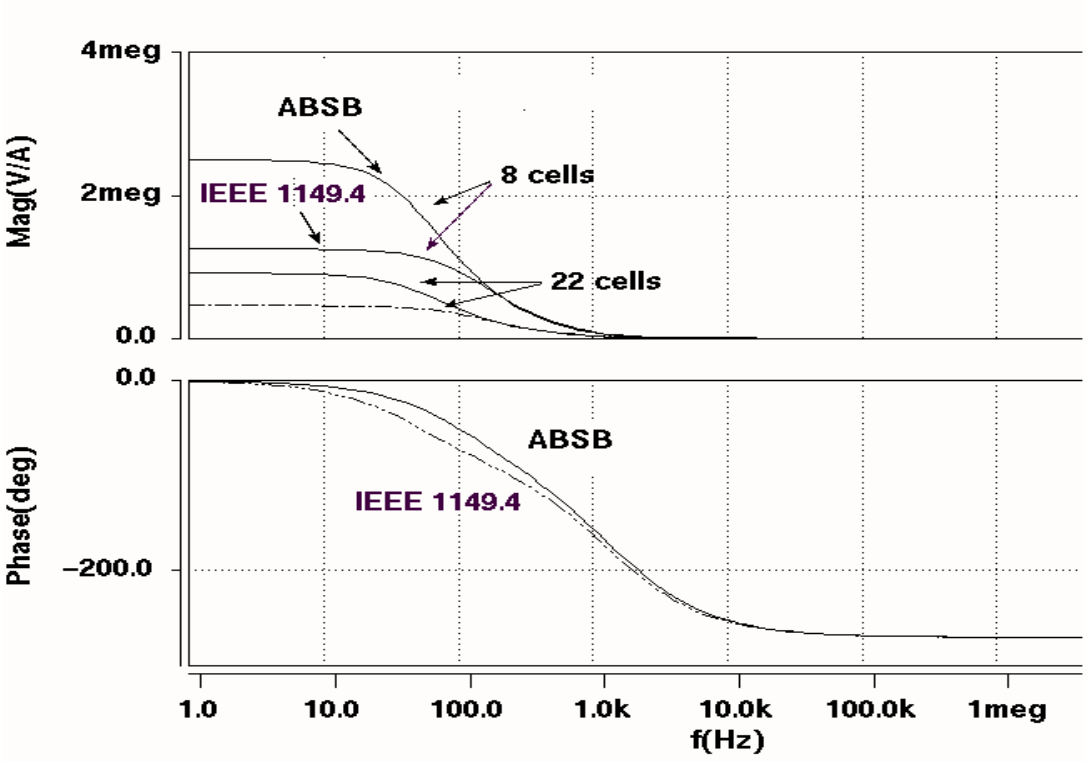

Figure 4.3.8 z_{12} parameters for IEEE P1149.4 and ABSB with 8 and 22 cells

Figures 4.3.7 and 4.3.8 can explain the effect of analog bus. When resistivity is measured, the characteristics of analog bus should be taken into account. For instance, if a resistor is to be measured, it should be aware that there is a resistor leakage in parallel with that resistor. Before any measurement is to be made, the analog test bus should be characterized and calibrated so that the loading effects could be minimized. The way to calibrate a test bus is not the objective of this thesis. However, it can be found in any literature about test instrument.

Chapter 5 Conclusion

This dissertation discussed means and techniques to improve mixed-signal testing of analog integrated systems in industrial environment. It covered a number of practical techniques from component verification, statistical fault detection, and optimum test point selection to innovative ways of using the IEEE boundary scan techniques.

A method to perform the equivalent of In-Circuit Test (ICT) as part of the End-Of-Line (EOL) Test during manufacturing of modules has been investigated. The experiments showed that the ICT stage in a manufacturing line can be effectively eliminated by component verification approach. This is important as the future modules are expected to pose access problems for the probes in ICT testers. A DFT rule was presented to complimentary the component verification method. The pull up resistor circuitry measurement can be used in some cases to calculate component values. However, some circuitry does not have this kind of structures. Therefore, these two methods can be used when necessary.

A procedure to test analog circuit using the combination of spectrum estimation and MD was proposed. The proposed method can be automated in performing fault simulation and in construction of the fault dictionary. It provides a robust statistical model for fault detection with good separation property and simplified representation. The frequency application uses a proper metric to measure the characteristics of analog frequency response. The advantages of doing so are the better separation of fault and easiness of programming. The AR model in the time domain essentially accomplishes a frequency sweep up to two

times the sampling frequency. It also reduced the dimension of the MD measures.

To select optimum test points, a fast algorithm for test point selection is proposed. The proposed approach is based on the entropy measure. It provides an algorithm faster than previously developed approaches and has fewer selected nodes than most of them. As a result a fault dictionary can be built with fewer number of test measurements needed to identify the fault. The selection method is applicable for other applications, in which a quality of selection can be established using system entropy, for instance in information systems [ZIA94]. In order to verify the quality of the results obtained a program to generate all test points was written. This program called REDUCT is based on the rough set theory and finds a minimum reduct by the expansion of discernability function.

Compared with the available techniques such as inclusive and exclusive test point selection, the proposed method very effectively finds a local minimum for the number of test points needed to isolate the faults. Future work will include Monte Carlo analysis and statistical methods to construct the fault-wise table and to perform the test point selection.

The feasibility study of using digital sequence in analog components testing has been conducted and results are presented. The analog information can be stored in a sequential digital registers and be shifted out for evaluation. Combining digital signature generation with neural network approach, we can deal with component tolerances in manufacturing testing. As companies try to integrate the analog functions into integrated circuits as much as possible, there are less and less analog components on a board. Still some analog components like the EMC (Electromagnetic Compatibility) protection capacitors and pull

up resistors are inevitable in the near future. The proposed methodology has special practical value in testing those limited analog components on PCB board along with IEEE std. 1149.1. In order to overcome the difficulties in waveform design, a pseudo random sequence is used as the digital input to an analog CUT and generates an analog output. The analog signal can be transformed into digital forms by D flip-flops using delay test concept. Then, the digital sequence can be shifted out through boundary scan cell for evaluation.

Finally, an analog boundary scan (ABS) bus has been proposed for observing analog function blocks. The proposed ABS can be used as a subset of IEEE P1149.4 for virtual probe. The proposed ABS is compared with IEEE P1149.4 by simulation examples. It is concluded that boundary scan bus has its limitation for high frequency applications. Without calibration of IEEE P1149.4 standard bus, the test cannot be precise. The future work should include a systematic way or metrology to use IEEE P1149.4.

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