A DECOMPOSITION METHOD FOR ANALOG FAULT LOCATION

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ABSTRACT

In this paper, fault location in large analog networks by decomposition method is generalized to include subnetworks not explicitly testable. Assume that the network topology and nominal values of network components are known and the network-under-test is partitioned into subnetworks once for all. The decomposition nodes could be either the accessible nodes whose nodal voltages can be measured or the inaccessible nodes whose nodal voltages under faulty condition can be computed by a new method proposed in this paper. The new method reduces the test requirements for the number of accessible nodes and increases the flexibility of decomposition. Location of faulty subnetworks and subsequent location of faulty components are implemented based on checking consistency of the KCL equations for the decomposition nodes and using ambiguity group location techniques. This method can be applied to linear or non-linear networks, and is particularly effective for the large scale analog networks. An example circuit is provided to illustrate the efficiency of the proposed method.

1. INTRODUCTION

With the development of modern computer-aided design and semiconductor integration techniques, such products as mixed-signal systems and system-on-chip (SoC) gained widespread applications in the area of multimedia, real-time control, wireless communication, and neural networks. Consequently, efficient and highly automated test paradigms are expected to benefit the design process and manufacturing yield. Traditionally, testing of mixed-signal system and SoCs adopt the decomposition method to partition the whole system into mechanical, software, analog, and digital subsystems in order to apply their domain specific test techniques. Finally system level test and interconnection test are applied to fulfill the testing task for the whole system.

Among these subsystem testings, analog testing is the bottleneck due to the inherited features of analog networks such as component tolerance, nonlinearity and lack of efficient fault models. Research efforts on analog test and fault diagnosis were summarized in [1-3]. Many testing techniques were developed and can be classified as verification, approximation, parameter identification and dictionary methods [1]. Facing up the practice of increasing scale of today's analog networks, design verification based on decomposition method is the best candidate for verification of large-scale analog networks. The most promising advantage of the decomposition method is that there is no upper bound for the number of faulty components in the network which exists in other verification methods. Another advantage is to reduce the test cost for large-scale network because only very limited number of faults occur in practice. After decomposition, fault-free subnetworks usually occupy a large portion of the complete system. Therefore the entire testing effort can be devoted to the faulty subnetworks. In [4], a method was designed to identify the faulty subnetworks under a nodal decomposition strategy. It is based on checking the voltage consistency of internal nodes in analyzed subnetworks. In decomposition method described in [5], faults are localized to within the smallest possible subnetworks according to the hierarchical decomposition structure. Because the measurement nodes are chosen as the nodes of decomposition, many accessible nodes are needed in order to locate the faulty components or faulty regions within the small subnetworks. Simultaneously, the fact that only accessible nodes could be decomposition nodes restricts the decomposition flexibility. Such requirement is not acceptable for today's analog networks whose scale is steadily increasing while the accessibility of the network nodes is decreasing. To achieve more information about the faulty components or faulty regions, there must be a compromise between the number of accessible nodes and the size of subnetworks. A new method is proposed in this paper to alleviate this problem in order to face up today's practice. Based on the network topology and checking consistency of the KCL equations, the nodal voltages of part of inaccessible nodes under faulty conditions could be computed. Hence, these computed nodal voltages can be treated as measurements and subsequently be used for decomposition. For the analog networks with sufficient accessibility, this method can reduce the measurement cost. For the analog networks with limited accessibility, this method can create more decomposition nodes and can increase the decomposition flexibility. An efficient solution to verification of decomposed subnetworks is based on recently developed method for finding ambiguity groups and solving ambiguous equations [6-7].

2. LOCATION OF FAULTY SUBNETWORKS IN ANALOG NETWORKS

There are two assumptions for the proposed method. The first one is that network topology and nominal values of network components are known, thus all the nodal voltages, branch currents and network parameters information are known before testing and such computations can be carried out off-line. The second one is that all of the partitioned subnetworks should be mutual coupling free. Let us begin with an important assumption used by decomposition method presented in [5] which will be alleviated by the method proposed in this paper: **all the decomposition nodes should be accessible to voltage measurements**. For the network-under-test some subnetworks are fault-free, some are faulty. It is easier to locate the fault-free subnetworks than the faulty subnetworks according to Lemma 1-3 in [5]. The first step of our method is to locate as many as possible fault-free subnetworks based on the following corollary which is derived from Lemma 2 in

[5]. In this paper a **common node** is defined as a node incident to several subnetworks in decomposed network or a voltage measurement node.

Corollary 1:
Suppose that a common node c is connecting k subnetworks S_i (i=1, 2, …, k). If all the currents incident to the common node c computed by the measured voltages and the nominal parameter values satisfy the KCL equations, i.e.,

$$\sum_{i=1}^{k} I_c^i = 0 \quad \forall t \tag{1}$$

$$I_c^i = h_c^{M_i}\left(v^{M_i}(t),\ f_i^0\right) \tag{2}$$

where I_c^i is the current incident to node c from subnetwork S_i, M_i is the measurement set consisting of measurement nodes, v^{M_i} are the measured nodal voltages in subnetwork S_i, f_i^0 are the nominal component values of subnetwork S_i, then all subnetworks S_i (i=1, 2, …, k) are fault-free.

Such common node is called **fault-free node**. If equation (1) is not satisfied then at least one subnetwork S_i is faulty. In this corollary, all decomposition nodes are measurement nodes.

Suppose now that one decomposition node x in subnetwork S_i is inaccessible, i.e., the node x is still the decomposition node but its nodal voltage V_x is unknown. Thus, the decomposed subnetwork topology remains unchanged, while the measurement set of S_i is changed by removing node x. We can still compute I_c^i in (2) by changing the measurement set as above. The Corollary 1 is still valid to locate the fault-free subnetworks.

Corollary 2:
Suppose an subnetwork S_i has two fault-free nodes y and z and one of the voltages V_x in this subnetwork is unknown. If the currents incident to these common nodes satisfy the KCL equations, i.e.,

$$\sum_{i=1}^{k_c} I_c^i = 0 \quad \forall t \quad c \in (y, z) \tag{3}$$

$$I_c^i = h_c^{M_i+X}\left(v^{M_i+X}(t),\ f_i^0\right) \tag{4}$$

where k_c is the number of subnetworks incident to common node c, then all subnetworks incident to nodes y and z are faul- free.

Here, the measurement set M_i is appended by node x. Since there is only one unknown variable V_x in (4), V_x can be determined uniquely because we know such solution exists in network-under-test. As a generalization of Corollary 2 we can formulate the following lemma.

Lemma 1:
Consider a subset of fault-free nodes in subnetworks S_i with p inaccessible decomposition nodes. All p nodes are appended to the measurement set, thus leading to p unknown variables V_{x1}, V_{x2}, …, V_{xp}. If there are m fault-free nodes and $m \geq p$, then by using m KCL equations

$$\sum_{i=1}^{k_x} I_x^i = 0 \quad x = 1, 2, ..., m \quad \forall t \tag{5}$$

$$I_x^i = h_x^{M_i+P}\left(v^{M_i+P}(t),\ f_i^0\right) \tag{6}$$

where k_x is the number of subnetworks incident to node x. We can determine all the voltages V_{x1}, V_{x2}, …, V_{xp} and verify that all the subnetworks incident to fault-free nodes are fault-free.

Using Corollaries 1 and 2 and Lemma 1 fault free subnetworks can be sequentially verified and internal voltages determined. The network in Figure1 is used to illustrate the process.

Example 1

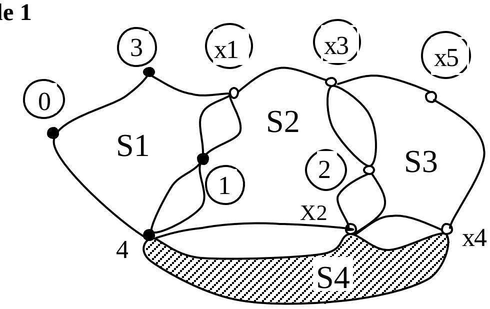

Figure 1 Decomposed network for example 1.

The network is decomposed into 4 subnetworks *S1*, *S2*, *S3*, and *S4*. Assume that *S4* (illustrated by the hashed area) is the only faulty subnetwork. Thus, nodes {0, 1, 2, 3, x1, x3, x5} are fault-free nodes whose node indexes are circled in Fig.1. Nodes 0 to 4 are accessible nodes and nodes x1 to x5 are inaccessible. Apply (3) to nodes 0 and 3 to compute the currents I^{S1}:

$$I^{S1}_{node\ 0} = h^{M_{S1}+X1}_{node\ 0}\left(v^{M_{S1}+X1}(t),\ f^0_{S1}\right) \tag{7}$$

$$I^{S1}_{node\ 3} = h^{M_{S1}+X1}_{node\ 3}\left(v^{M_{S1}+X1}(t),\ f^0_{S1}\right) \tag{8}$$

where the measurement set is M_{s1} =[node0, node1, node3, node4]. Currents computed from (7) and (8) should be either zero or equal to external current excitations at these nodes. Then *S1* is concluded as fault-free by Corollary 2 and internal voltage V_{x1} is calculated.

Subsequently by applying Lemma 1 to fault-free nodes in subnetworks S_2 and S_3, (nodes 1, 2, x1, x3, x5) with inaccessible decomposition nodes x2, x3, x4, and x5, 5 equations are obtained with 4 unknown voltages. We can determine the unknown voltages V_{x2}, V_{x3}, V_{x4}, and V_{x5}, as well as verify that *S2* and *S3* are fault-free.

The results obtained by using Lemma1 require knowledge (or a guess) of fault-free nodes, since only KCL equations in these nodes can be used to formulate the verification equations. Instead of this ad-hoc approach, subnetwork verification can proceed efficiently using recently developed methods for finding ambiguity groups and solving ambiguous equations.

3. FAULT LOCATION AND VERIFICATION

We propose a method for the location of fault-free nodes and their verification for a linear network with N nodes, M measurement nodes and F faulty nodes. We assume that $M>F$. The network nodal equations can be formulated as follows

$$T_0 \begin{bmatrix} V_M \\ V_{N-M} \end{bmatrix} = [W_0] + [W_F] \tag{9}$$

where T_0 is the nominal multiterminal matrix of the decomposed network (size equal to the number of decomposition nodes) , V_M and V_{N-M} are measured and unknown decomposition node voltages respectively, W_0 is known excitation vector, and W_F is unknown vector of faulty sources at faulty nodes.

Since, in general, location of fault-free nodes is unknown we need to determine the unknown voltages, identify fault-free nodes and verify fault-free equations. To this end let us first modify (9) as follows

$$T_1 V_M + T_2 V_X = [W_0] + [W_F] \tag{10}$$

$$T = [T_1 \quad T_2] \tag{11}$$

and move the first term from the left-hand side to the right-hand side and combine it with the right-hand side vector to get

$$T_2 V_X = [\hat{W}_o] + [W_F] \tag{12}$$

where
$$[\hat{W}_o] = [W_0] - T_1 V_M \tag{13}$$

is a known vector. Let us formulate the ambiguity group matrix

$$B = [T_2 \quad \hat{W}_0] \tag{14}$$

This matrix has N rows and N-M+1 columns.

Since the entries in vector W_F corresponding to faulty nodes are nonzero while the entries corresponding to fault-free nodes are zeroes, N-F equations can be obtained from (12) with N-M unknowns if we know the exact location of faulty nodes. Hence, the unique solution to all V_X can be determined. To avoid a combinatorial search for faulty nodes, a recently developed ambiguity groups locating technique can be utilized to efficiently locate all fault-free nodes [6-7]. It is based on QR factorization to find a numerically stable solution of over determined system. The primary idea is to find dependent relationship among the rows of matrix B, that is, to identify the ambiguity groups in (12) with the maximum size. The QR factorization and swapping is applied together with corresponding theoretical results described in [6-7]. A new lemma is proposed below to locate the maximum number fault-free nodes.

Lemma 2:
If $M>F$ and matrix B has full column rank ambiguity group then the row indices of the submatrix which form this ambiguity group are fault-free nodes and all the subnetworks incident to these nodes are fault free.

Example 2

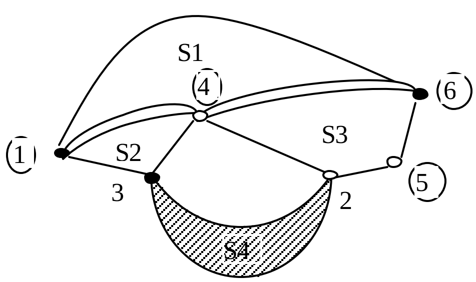

Figure 2 decomposed network for example 2

Example 2 is provided to illustrate the location of fault-free nodes. The network has 6+1 nodes with one of nodes being reference. The measurements are taken on nodes {1, 3, 6} which are black points in Figure 2 and the fault-free nodes are nodes {1, 4, 5, 6} whose indexes are circled. The parameters are as below:

$$T_0 = \begin{bmatrix} 1 & 0 & 5 & -2 & 0 & 6 \\ 0 & 2 & 0 & 7 & 9 & 3 \\ 5 & 0 & 3 & -1 & 0 & 0 \\ -2 & 7 & -1 & 4 & 7 & 8 \\ 0 & 9 & 0 & 7 & 5 & 7 \\ 6 & 3 & 0 & 8 & 7 & 6 \end{bmatrix} \quad W_0 = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad J_F = \begin{bmatrix} 0 \\ -2 \\ -3 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad V_M = \begin{bmatrix} V_1 \\ V_3 \\ V_6 \end{bmatrix} = \begin{bmatrix} -0.2455 \\ -0.4437 \\ 0.7245 \end{bmatrix}$$

By (14), *6x4* matrix B is obtained for analysis. Applying the ambiguity group locating techniques in [6-7], a *4x2* linear combination matrix C is obtained after QR factorization and column swapping as follows

$$C = \begin{bmatrix} -1.7500 & -1.0000 \\ -4.8869 & -4.0714 \\ 2.5357 & 1.7143 \\ 0.6667 & 0.0000 \end{bmatrix}$$

with its basis including nodes {5, 1, 4, 3} and co-basis nodes {2, 6}. The unique zero entry in C indicates that the ambiguity group {5, 1, 4, 6} is located and according to Lemma 2 contains fault-free nodes.

The above method to locate the fault-free nodes is based on linear nodal analysis, thus is only applicable to linear network. For nonlinear network, Lemma 2 can be used to implement the location of fault-free nodes with the incident current I_c^i computed by (2). Note that only measurement nodes should partition the nonlinear networks.

After location of fault-free nodes and faulty subnetworks, the computation efforts required by faulty component location are limited. Since there is no strict requirement for the memory and testing time in today's medium or small scale analog test, the choice for faulty component location techniques inside the faulty subnetwork is versatile such as the techniques provided in part V of [5] or the techniques provided by other references for linear analog networks [7-8] and for nonlinear analog networks [9].

For the linear network, equation (30) in [5] can be utilized to compute the external current. For the network with faulty nonlinear components, faulty model of nonlinear components can be utilized to locate the faulty nonlinear components. For the network with faulty linear components and fault-free nonlinear components, utilize nonlinear network solver such as Pspice to locate the faults.

4. EXAMPLE CIRCUIT

To illustrate the efficiency of the proposed approach and to compare the proposed method and the method in [5], the Example 5 in [5] is selected. Figure 3a is the first stage of the analog filter example circuit. The equivalent circuit for the operational amplifier is outlined in Figure 3b. The nominal circuit component values, the decomposition structure and indexes of subnetworks are the same as that illustrated in Figure 9 of [5].

The faulty components are *R15=0.2kW*, *R17=2.0kW*, *R27=11.14 kW*, and *C18=0.1mF* which lead to faulty nodes {8, 9, 10, 11, 12}. Measurement set is nodes {1, 3, 5, 10, 14, 17, 19, 37}. The unknown nodal voltages at nodes {6, 8, 12, 15} are to be solved by the proposed method and fault-free nodes determined. Hence, $N=37$, $M=8$, $F=5$ and $M>F$. The sinusoidal current source to node 1 is $j(t) = 0.01\cos(2000\,t)A$. Notice that with these limited measurements the method presented in [5] would not apply since there is no single fault free node with all incident subnetwork voltages measured.

The first step is to locate the fault-free nodes by the methods in Part 3. The *37x31* matrix B is constructed by network nominal values and measurement vector V_M. After QR factorization and swapping operations, a *31x6* linear combination matrix C is obtained. The ambiguity group located is {1--7, 13--37} which matches the fault-free nodes in real case. The second step is to decompose the network into subnetworks by measurement nodes plus nodes {6, 8, 12, 15}.

Applying Lemma 1 to fault-free nodes {1, 3, 5}, we can obtain 3 equations with 2 variables V6 and V8 as follows

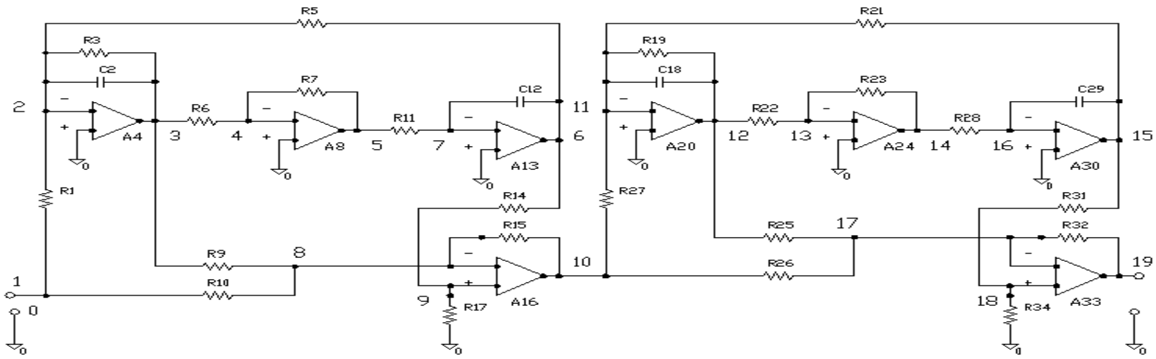

Figure 3a. Active low-pass filter

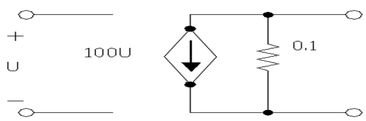

Figure 3b Model of OPAMP.

$$0=I_1^{S6}+I_1^{S15}+J$$
$$=\left(-8.519e-3+7.236e-4i+V6(-3.197e-4+9.821e-7i)\right)$$
$$+\left(-9.848e-3+7.867e-7i+V8*(-9.009e-5)\right)+(1.000e-2)$$
$$0=I_3^{S6}+I_3^{S12}+I_3^{S14}$$
$$=\left(-1.415e+2+1.228e+1i+V6*(-5.818+1.787e-2i)\right)$$
$$+\left(-1.049e-5-1.284e-4i\right)+\left(6.462e-5-1.834e-5i\right)$$
$$0=I_5^{S12}+I_5^{S13}$$
$$=\left(-4.072e-5-4.865e-4i\right)$$
$$+\left(-2.551e-5+3.446e-6i+V6*(-1.053e-6-1.994e-5i)\right)$$

After solving and verifying, the solution vector is

$$[V_6\ V_8]=[-24.329+2.0362i \quad -6.5672+0.54964i]$$

Similarly, by applying Lemma 1 to fault-free nodes {14, 17, 19} we can obtain 3 equations with 2 variables V12 and V15 and the solution vector is

$$[V_{12}\ V_{15}]=[\ 6.912e-3+6.629e-2 \quad 1.429-1.522e-1i]$$

According to Lemma 1, subnetworks {S9, S16} are declared as faulty. To locate and verify the faulty components, we utilize the techniques in [7]. The faulty components are declared as {R15, R17, R27, C18} which are the exact answer.

5. SUMMARY

Analog test and fault diagnosis is an important topic in the area of test and testability. To address the testing problem in large-scale analog networks that dominate the market of mixed-signal products or SoC products in recent years, fault location by decomposition method is generalized in this paper. The network topology and nominal component values are available before testing. The decomposition of the network into subnetworks is implemented and ambiguity group finding technique is used to locate fault-free decomposition nodes. While in the former research only the accessible nodes can be the decomposition nodes and decomposition is hierarchical, in this paper the inaccessible nodes can be the decomposition nodes as well and decomposition is implemented all at once. A new method proposed in this paper computes their nodal voltages under faulty condition. The benefits resulting from this work include reduction of the test requirements for the number of accessible nodes and increase in the flexibility of decomposition. By checking consistency of KCL equations for the decomposition nodes, faulty subnetworks and the subsequently faulty components can be located. Testing conditions are independent of the network and excitation types, thus the method is applicable to both linear and nonlinear networks, and to both time domain and frequency domain. The proposed method is particularly effective for the large-scale analog networks. The same example circuit as that in former research is utilized to demonstrate the efficiency of the proposed method.

6. REFERENCES

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