A Novel Low-Power Logic Circuit Design Scheme

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***Abstract*—This brief proposes a novel low-power digital logic design scheme based on the energy exchange in the switched inductor–capacitor (S*LC*) circuit. It presents a design paradigm which in ideal case may lead to a circuit capable of performing logic operations with no switching losses. In traditional integrated circuit design, the energy is stored in the output load capacitor through a pull-up path (corresponding to storing a logic 1). When the output changes its logic value, this stored energy is dissipated through the pull down path to the ground. In order to reduce this switching energy dissipation each time the load capacitor is discharged, we store its energy in the magnetic field of the inductor in the proposed S*LC* architecture. Whenever the output load needs to be charged again, we transfer the energy back from the inductor to the load capacitor. This significantly reduces the switching energy. We illustrated the operation of the S*LC* architecture through SPICE simulation. A brief discussion of some practical considerations for this architecture is also presented.**

***Index Terms*—Buses, clock distribution tree, logic design, low power, switched inductor–capacitor (S*LC*) circuit.**

I. Introduction

LOW-POWER design is one of the most critical issues facing nanometer very large scale integration (VLSI) circuit design. With the continuous scaling of the technology, the power consumption has become a bottleneck for widely used high-speed, battery powered portable devices. It is the aim of this brief to present a novel low-power logic design scheme based on the switched inductor–capacitor (S*LC*) architecture.

Power dissipation in a CMOS-based logic circuit is dominated by the switching energy [1], [2]. This is the energy that must be dissipated in order to change internal state of the devices. Other sources of energy loss in CMOS circuit are related to leakage current [3]–[5] and to the short-circuit current [2], [6]. While the other two types of energy loss can be reduced to arbitrary low levels (at least in theory) by regulating the voltages levels (both power supply and thresholds), there seems to be no solution to eliminate dynamic power dissipation.

Since dynamic power is the dominant component of the CMOS power consumption, an extensive research effort is focused on the dynamic power reduction. Reference [1] addressed the problem of minimizing dynamic power consumption in synchronous sequential designs. The proposed method first applies a guided retiming and then applies supply voltage scaling on the retimed design. Experimental results show that the proposed approach can reduce dynamic power consumption by as much as 61%. Reference [7] proposed a novel multiple-output low-power architecture of linear feedback shift register (LFSR) design. Simulation results on a 0.18-μm technology show that this architecture can reduce the dynamic power about 50% compared to the traditional LFSR. Reference [8] proposed a design of low-power CMOS without level-shifters using dual threshold logic circuits. Simulation results show 20% and 17% savings for ISCAS'85 benchmark circuits designed with 180 and 70-nm technology, respectively. In [9], an exponentially tapered H-Tree clock distribution network was proposed to reduce dynamic power dissipation. Simulation results show this technique can reduce the dynamic power dissipation by 15%.

There is also an intensive research to reduce other sources of power dissipation indicating increasing importance of power management and low-power design. Reference [3] presented the leakage power characteristics of domino logic circuits with the consideration of the process parameter variations. In [4], a scheme based on the idea of gate-level restructuring and selective insertion of control points was proposed to reduce the leakage power. Simulation results show an averaged 67% of leakage reduction for the ISCAS'85 benchmark. For short-circuit power reduction, [10] discussed the use of on-chip inductance to improve the signal slew rate, therefore reducing the short-circuit power consumption.

In this work, we propose a novel computing paradigm, that in ideal case, may lead to logic operations without dynamic power dissipation. The solution proposed is a theoretical one, since so far no practical devices were build to support this kind of circuits. However, lowering the path resistance by several orders of magnitude is certainly within the reach of superconducting devices, thus the proposed paradigm may become a valuable solution for future technologies. To our best knowledge, there is no such digital logic scheme reported in literature yet.

Logic operations of circuits discussed in this brief can be performed by using two types of switches. The first type of switch is on or off depending on the strength of electric field, similar to MOS switches. All simulation results presented in this brief refer to this type of switches. However, it would be equally easy to develop a dual approach in which switches would be on/off depending on the strength of the magnetic field, since in our work the energy is stored both in electric field of a load capacitor or in the magnetic field of the load inductor.

This brief is organized as follows. Section II presents the basic idea of the proposed architecture, detailed discussion of the S*LC* architecture and its operation phases. In Section III, SPICE simulation of the proposed architecture is given. Detailed discussion about the construction of various logic gates, including inverting and noninverting logic gates, and energy loss analysis of S*LC* circuit are presented in this section. In Section IV, we gave a brief discussion of the related technological and timing issues

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as well as directions for future research. Finally, a conclusion is given in Section V.

II. Low-Power S*LC* Architecture

The primary components of power dissipation in digital CMOS design can be estimated using [2]

$$\text{Dynamic power: } P_{\text{dyn}} = \alpha C_L V_{\text{DD}}^2 f. \quad (1)$$

$$\text{Short-circuit power: } P_{\text{sc}} = t_{\text{sc}} V_{\text{DD}} I_{\text{peak}} f. \quad (2)$$

$$\text{Leakage power: } P_{\text{leakage}} = V_{\text{DD}} I_{\text{leakage}}. \quad (3)$$

In the above, α is the switching activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, f is the clock frequency, t_{sc} represents the time for short-path conducting from V_{DD} to ground and I_{leakage} is the leakage current.

Dynamic power is the dominant component among these three sources. Assume a logic gate is driving a load capacitor C_L. Each time when there is a logic 1 at the output, C_L is charged through the pull-up circuit from the supply voltage V_{DD}. This energy is stored in the capacitor until the output logic value changes to 0 and the load capacitor C_L is discharged. In this case, the stored energy will be dissipated through the pull down circuit to the ground. This energy is changed to thermal energy and needs to be removed by a cooling process. The amount of energy dissipated through switching the logic output value does not depend on the switch resistance. Even if superconducting switches were used it will remain on the same level. Not only this drains the battery power, it also creates a requirement for an efficient heat removal and increases the packaging cost.

An alternative approach would store this energy and re-use it whenever it is needed. Based on this idea, we propose a novel S*LC* logic architecture capable to operate without energy losses. In this architecture, the energy is stored alternatively in the inductor whenever the load capacitor C_L is discharged, and in the capacitor C_L whenever it needs to be charged again. In this way, ideally, no energy is wasted and we only need to charge the load capacitor once. In non-ideal devices, stored energy is reduced through leakage current or dissipated on path resistance (defined as a combination of switch resistance, serial resistance of inductor, capacitor or wires) and needs to be restored. This is discussed in detail in Section III-C.

The proposed architecture is especially suitable in the situation when a large load capacitor needs to be charged and discharged. Buses and clock distribution trees are two examples of such loads [11], [12]. For instance, it is reported that the bus dissipated about $15\% \sim 30\%$ of total power in Alpha 21064 and Intel 80386 [13]. In the second generation of the Alpha microprocessor Alpha 21164, the clock distribution tree consumes 20 W, which is 40% of the total power dissipation of the processor [14]. A simple S*LC* circuit may save most of this energy. The major difficulty to implement the proposed logic design scheme will arise from the fabrication process and implementation technology. We gave a brief discussion of these issues in Section IV.

Fig. 1 shows a basic logic gate structure of the proposed S*LC* architecture. It consists of a switch control unit (SCU) with two control signals *CS1* and *CS2* and two energy storage elements—inductor (L) and load capacitor (C). Inside the SCU,

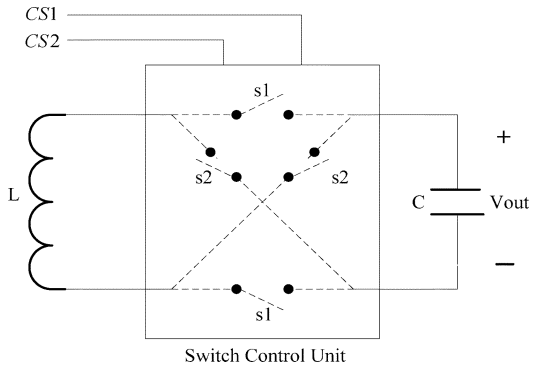

Fig. 1. Proposed S*LC* architecture for low-power design.

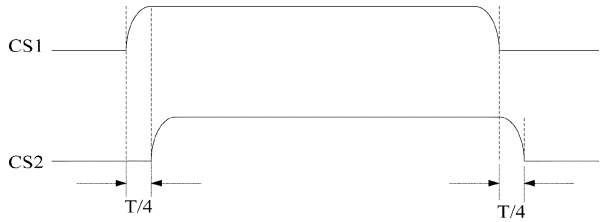

Fig. 2. Control signals of CS1 and CS2.

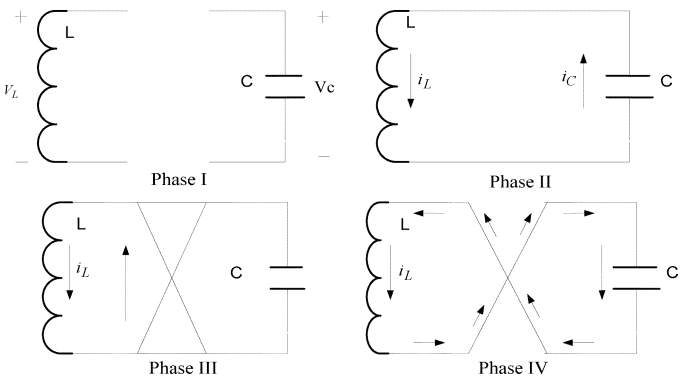

Fig. 3. Operation phases of the proposed circuit.

there are four switches controlled by two-phase control signals CS1 and CS2, which control switches *s1* and *s2*, respectively. If the control signal is equal to 1, the corresponding switch is on, otherwise it is off.

Circuit shown in Fig. 1 inverts the control input value, thus implementing an inverter. Unlike CMOS gates that implement inverting logic, this design style can produce both inverting and noninverting logic in the same circuit. We now give a detailed description of this circuit work focusing on inverting logic operation first. Noninverting logic can be obtained by using complementary switches as discussed in Section III-B.

Fig. 2 shows the waveform of the control signals CS1 and CS2, where T is the period related to the *LC* resonant frequency: $T = 2\pi\sqrt{LC}$.

Based on the control signals CS1 and CS2 value, this circuit will have four phases of operation illustrated in Fig. 3.

A. *Phase I:* $\text{CS1} = 0$, $\text{CS2} = 0$

In this phase, switches *s1* and *s2* are off. Energy is stored in the load capacitor C. This corresponds to a logic 1 in the output load.

B. *Phase II:* CS1 = 1, CS2 = 0

In this phase, *s1* and *s2* switches are off. The stored energy in the capacitor C is transformed to the inductor L. The capacitor voltage and the inductor current are

$$v_c(t) = v_0 - \frac{1}{C}\int_0^t i(t)dt$$
$$i_l(t) = \frac{1}{L}\int_0^t v(t)dt. \quad (4)$$

After $T/4$, the capacitor voltage becomes 0 and the inductor current reaches the maximum point. At this moment, switches *s2* are closed (on) according to the control signal. This leads to the phase III.

C. *Phase III:* CS1 = 1, CS2 = 1

In this phase, all switches are on. The current is cycled in the inductor and the short-circuit paths. This will keep the capacitor voltage at 0, which corresponds to a logic 0 at the output load. The load energy is not lost in this phase as it is stored in the magnetic field of the inductor.

D. *Phase IV:* CS1 = 0, CS2 = 1

Whenever there is a need to re-charge the load capacitor again to switch the load output from 0 to 1, the switch *s*2 is set on and *s*1 is off. This will re-charge the load capacitor to the full voltage. After $T/4$, the capacitor voltage reach the maximum point and energy is restored in the electrical field of the capacitor. The inductor current is 0 at this point. Switches *s*2 then are open again (off), which leads to the initial phase I.

As we can see from the above analysis, the energy is stored in the inductor when there is a need for discharge the load capacitor. Whenever next time the capacitor needs to be re-charged, we can reuse the energy stored in the inductor. Ideally, no energy is lost in this architecture. The reason for the cross connection of the switches in the switch control unit is to avoid the negative charge on the load capacitor.

In summary, the circuit presented in Fig. 1 implements an inverter. Its output voltage stored on the capacitor follows changes of the inverted control input signals CS1 and CS2. While *CS*1 is an arbitrary input signal, CS2 is the CS1 signal shifted by $T/4$.

III. Simulation Results

In this section, we conduct SPICE simulation for Fig. 1 to build inverting and noninverting logics, and compare the energy loss of the proposed circuit with those of the traditional IC design.

A. *Inverting Logic Construction*

Various logic gates can be build using the described energy exchange and storage mechanism. To implement a general compound gate we use the same approach as in nMOS design. To accomplish a pull down operation (logic 0) we compose a conducting path of switches controlled by various input signals. A series connection of switches implements logic AND, while parallel connection implements logic OR. By properly combining switches controlled by the input signals, we can implement any logic function F in the pull down path. Thus, a switch controlled path implements a logic function F, and the resulting S*LC* gate implements this logic function inverse $\overline{F}$.

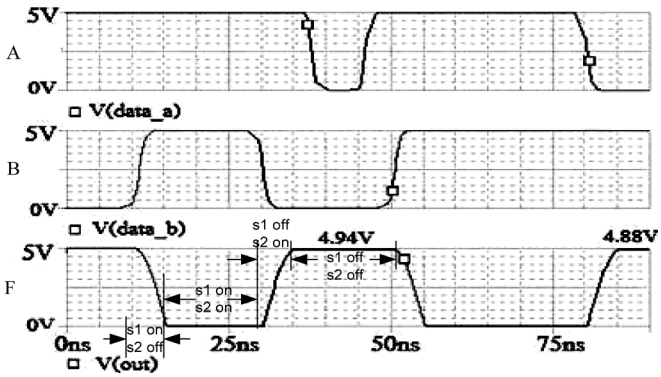

Fig. 4. $F = \overline{A \bullet B}$ output waveform.

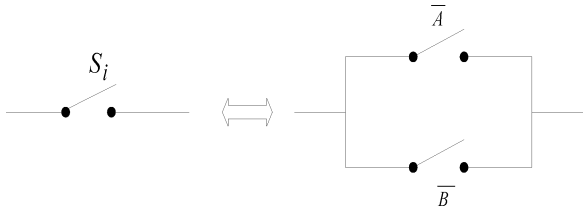

Fig. 5. Switch s_i replaced by path of complementary switches.

Assuming for instance that we want to construct the 2-input NAND gate $F = \overline{A \bullet B}$. To implement this function, each switch *s1* in Fig. 1 is replaced by a series connection of two switches controlled by signals A and B respectively. Each switch *s2* is replaced by a series connection of two switches controlled by signals A and B delayed by $T/4$. The $T/4$ delay can be achieved by passing the input signal through a transmission delay line. Fig. 4 shows the simulation result. As we can see, the logic function is correctly implemented and the four operation phases presented in Section II are clearly marked. Fig. 4 also shows that there are some energy losses when the load capacitor is re-charged back from the inductor (the output voltage drops from 5 V at the beginning of simulation to 4.94 and 4.88 V in the first and second re-charge period, respectively). This voltage drop is due to the path resistance. We need to periodically re-charge the output capacitor through the pull-up path when the stored energy is below a set threshold. The energy losses of the S*LC* scheme is discussed in detail in Section III-C.

B. *Noninverting Logic*

Unlike CMOS circuits that implements inverting logic only, the proposed S*LC* structure can be used to build noninverting logic. This can be accomplished by using complementary switches in the switch control unit. The complementary switch is on when the control signal is 0 and is off, when the control signal is 1.

In this case, the conducting path must stay open to maintain the high output value, so we must express the complemented function value through a logic combination of complemented input signals. For instance to obtain a 2-input AND operation, we build a conducting path of complementary switches connected in parallel (Fig. 5) that implements $\overline{F} = \overline{A} + \overline{B}$ (equivalent to $F = A \bullet B$).

Notice that, if the parallel connection of regular switches is used, the same S*LC* circuit would implement a NOR gate $F = \overline{A + B}$.

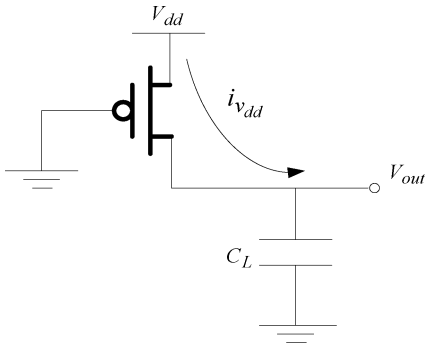

Fig. 6. Equivalent circuit in the charging load capacitor phase.

C. Energy Loss Analysis

Fig. 6 shows an equivalent circuit to charge the load capacitor from 0 to $V_{\rm dd}$ in the traditional IC design.

The energy taken from the supply during the charging transition $E_{V_{\rm dd}}$ and the energy stored in the load capacitor at the end of the transition E_C are [2]

$$\begin{aligned} E_{Vdd} &= \int_0^\infty i_{V_{\rm dd}}(t) V_{\rm dd} dt \\ &= V_{\rm dd} \int_0^\infty C_L \frac{d_{v_{\rm out}}}{dt} dt \\ &= C_L V_{\rm dd} \int_0^{V_{\rm dd}} dv_{\rm out} \\ &= C_L V_{\rm dd}^2 \end{aligned} \tag{5}$$

$$\begin{aligned} E_c &= \int_0^\infty i_{v_{\rm dd}}(t) v_{\rm out} dt \\ &= \int_0^\infty C_L \frac{dv_{\rm out}}{dt} v_{\rm out} dt \\ &= C_L \int_0^{V_{\rm dd}} v_{\rm out} dv_{\rm out} \\ &= \frac{C_L V_{\rm dd}^2}{2}. \end{aligned} \tag{6}$$

As we can see from (5) and (6), half of the energy is dissipated in the transition regardless of the size of the pMOS device and its effective resistance. During the discharging phase, the stored energy $C_L V_{\rm dd}^2/2$ will be dissipated through the nMOS device to the ground. Thus, with each change of the logic value this device dissipates E_C energy.

However, this is different in our proposed S*LC* circuit. Fig. 7 shows the relationship between the percentage of stored energy losses per cycle with respect to the path resistance for different *L* and *C* values. The x axis is the value of the path resistance (in ohms) and y axis is the percentage of energy losses. As we can see, the energy loss increases with the increase of the path resistance. We need to periodically recharge the output node through the pull-up path when the output voltage is lower than some threshold. Assume we set this threshold to $V_{\rm dd}/2$, which corresponds to the loss of 75% of the energy stored in the output capacitor. This 75% threshold line determines the maximum value of the path resistance. Fig. 7 also shows that to get the optimal energy saving performance, we need to fabricate very low resistance switches (below 10 Ω for this circuit parameters).

Path resistance affects not only the energy loss but frequency of operation of S*LC* circuit as well. As we can see from Fig. 7,

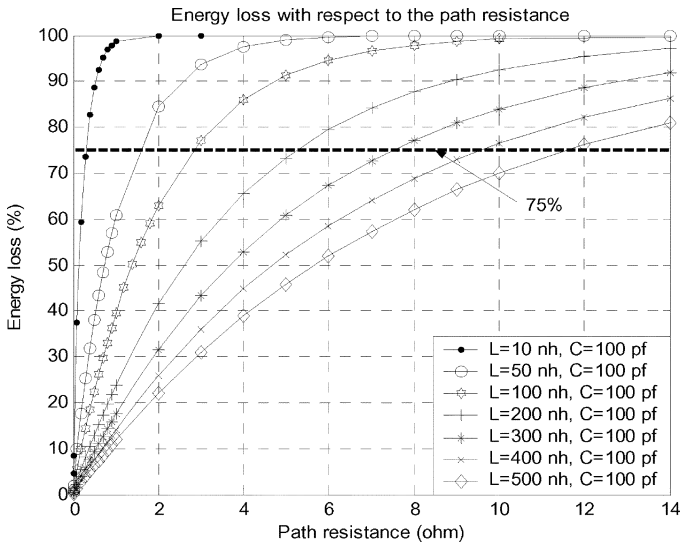

Fig. 7. Energy loss with respect to the path resistance.

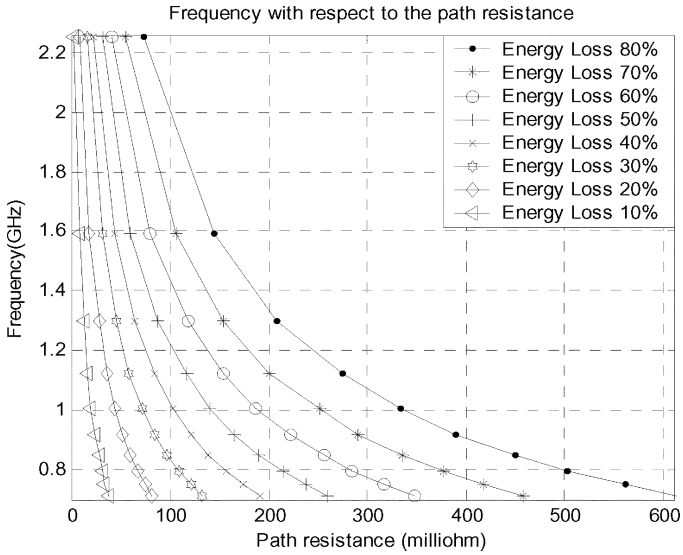

Fig. 8. Frequency relationship with the path resistance.

the larger the path resistance, the larger the inductor value that corresponds to the same level of energy loss. This in turn means that the larger the resistance, the smaller the operating frequency. Fig. 8 shows the *LC* resonance frequency with respect to the path resistance for different energy loss levels.

There are two time periods in the S*LC* circuit: Period T is decided by the resonance frequency of the *LC* parameters and sets $T/4$ delay of CS2 signal with respect to the CS1 signal (Fig. 2). The other period T_f is related to the operation frequency of the logic function. T_f must be significantly larger than T to guarantee that the logic function is correctly implemented. For instance, consider the 40% energy loss line in Fig. 8. If the path resistance is about 100 mΩ, then the resonance frequency is about 1 GHz. If we set the logic operation frequency to be ten times lower than this resonance frequency, then the maximum logic operation frequency is 100 MHz. With further reduction of the path resistance, the logic operation frequency will increase. Though fabrication of low-resistance switches is not practical in the current technology, lowering the path resistance to single milliohms could be within reach of superconducting devices in

the future. Therefore, the speed of the S*LC* circuits should satisfy the requirements of the modern digital circuits.

IV. Discussion and Future Research

In this brief, we presented the idea of the low-power digital design based on the proposed S*LC* architecture. Simulation results show correct behavior of the proposed logic. However, for this methodology to be used in practical nanometer IC design, there are several issues that need to be carefully evaluated and require further research.

1) Area overhead. Generally speaking, a proposed S*LC* gate needs two times the number of the transistors plus an inductor than the equivalent CMOS gate. The proposed scheme is especially suitable for the circuits which need to drive large capacitive loads, such as buses and clock distribution tree, or in the situation when power consumption is the most critical concern with no strict limitation on the design area.
2) Since the path resistance will consume some energy, therefore we need to periodically recharge the load capacitor through pull-up path when it is lower than some pre-set threshold. This would require extra circuitry. In addition to meet the speed requirements of the modern digital circuit, the switched on resistor should be on the level of miliohms or less. This is out-of reach of current MOS technology.
3) This new circuit needs the fabrication of accurate on-chip accurate inductors. This presents a serious challenge for the fabrication technology. For reference please review the practical design considerations for on-chip inductor presented in [15], [16]. In [15], the impact of interconnect scaling, copper metallization and low-K dielectric on the achievable inductor quality factor is studied. In [16], the design criteria and processing techniques for designing of on-chip inductors up to 5 GHz is discussed.
4) The correct operation of this circuit depends on proper timing of the control signals. Control signal 2 is a control signal 1 delayed by a quarter of the *LC* oscillation period. How to provide this accurate delay time is also a design challenge. One way to alleviate this problem is to use clocked gate operations, in which all switched paths will contain a clock control switch for synchronization of the control signals.

Explorations of superconductor properties to digital computing are subject of intensive research. Perhaps the most promising technologies today explore superconducting quantum computing circuits [17] and superconducting properties of nanowires [18]. None of these techniques however, considers energy transfer from magnetic to electric field which is a basis of the computing model developed in this brief.

V. Conclusion

In this brief, we presented a novel low-power logic circuit design scheme based on the S*LC* architecture. In the proposed circuit, the energy is stored in the inductor whenever there is a need for the load capacitor to be discharged. This stored energy is used to re-charge the load capacitor whenever it needs to be charged again. Therefore, the dynamic energy consumption is significantly reduced. We illustrated the operation of the proposed architecture through SPICE simulation with the consideration of path resistance. The proposed architecture is especially suitable for the circuits which need to drive large capacitive loads, such as buses and clock distribution trees. Series practical issues would have to be addressed for this architecture to be used in digital designs, such as nonideal components, time control of the delay signals, and fabrication of the accurate inductors. A brief discussion of these issues are presented.

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