Low-Power Tunable Analog Circuit Blocks Based on Nanoscale Double-Gate MOSFETs

Savas Kaya, *Senior Member, IEEE*, Hesham F. A. Hamed, and Janusz A. Starzyk, *Senior Member, IEEE*

***Abstract*—We illustrate unique examples of low-power tunable analog circuits built using independently driven nanoscale DG-MOSFETs, where the top gate response is altered by application of a control voltage on the bottom gate. In particular, we provide examples for a single-ended CMOS amplifier pair, a Schmitt Trigger circuit and a operational transconductance amplifier C filter, circuit blocks essential for low-noise high-performance integrated circuits for analog and mixed-signal applications. The topologies and biasing schemes explored here show how the nanoscale DG-MOSFETs may be used for efficient, tolerant and smaller circuits with tunable characteristics.**

***Index Terms*—Integrated circuits, tunable analog circuits, mixed-mode simulations, DG-MOSFET.**

I. Introduction

IN THE FINAL stretch of the CMOS downscaling trend, projected to reach the 22-nm limit by 2010 [1], double-gate (DG) MOSFET architectures on system-on-insulator (SOI) substrates are expected to replace the traditional bulk device structures [2], [3]. While multi-gate SOI structures are ideal for digital performance, they will be also strong contenders for analogue RF applications in lucrative wireless communications market due to their ability to effectively handle gigahertz modulation, to minimize parasitics via low-loss substrate and to cross-modulate double gates through thin silicon body. However, the actual potential of DG-MOSFETs have not been assessed in detail and there is a clear gap in the literature with regards to analog circuit applications [4]. Hence, it is imperative to explore this gap, surveying and exploiting unique features of DG-MOSFETs especially for specific RF signal processing tasks [5], [6].

A particularly attractive possibility for analog circuit applications is the tunability of DG-MOSFETs' front-gate functionality via bottom (back) gate bias [7], [8]. This has a number of important implications for circuit design: 1) increased functionality out of a given set of devices; 2) reduction of parasitics and layout area; 3) higher speed operation and lower power consumption with respect to equivalent conventional circuits. Although several works that utilizes DG-MOSFETs in RF mixing applications have been published so far [7]–[9], the tunability of the DG-MOSFETs have been largely ignored by the analog designers. Most of the existing works on the analog performance of DG-MOSFETs [10], [11] concentrate on the individual device figures of merit such as g_m/I_d characteristics, power [10] and cutoff frequency [11] and linearity [5], showing its superiority in terms for low power, speed, and signal integrity. In this brief, however, we focus on the circuit applications, exploring simple analog circuit blocks built using DG-MOSFETs, in which bottom gate is used to tune the circuit performance. We show how compact low-power circuits including single-ended amplifiers, Schmitt Trigger blocks and differential operational transconductance amplifiers (OTAs) may be built and tuned using TCAD simulations. Thus, we attempt to provide a valuable insight into novel analog design strategies and circuits based on DG-MOSFETs optimized normally for digital applications.

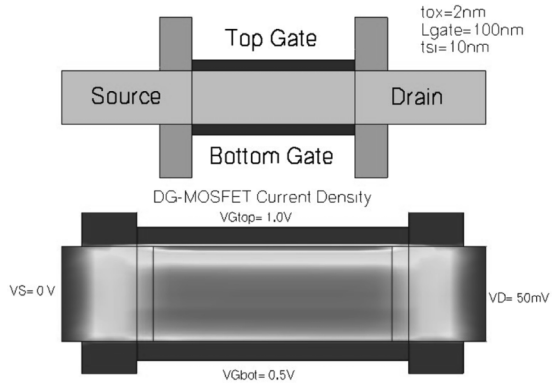

Fig. 1. DG-MOSFET device structure (top) used in this work has the gate length $L_g = 100$ nm, body thickness $t_{\rm Si} = 10$ nm, and oxide thickness $t_{\rm Ox} = 2$ nm, which reflect typical values for digital applications. DESSIS device simulator is used in the mixed-mode simulation mode [13] and drift–diffusion approximation is employed to reduce the computaional cost. Current density distribution at an asymmetric bias condition is shown above, where the top channel is fully switched on.

II. Device Structure and Modeling

DG-MOSFETs considered in this work are chosen to facilitate the mixed-mode circuit design methodology, which seeks to integrate analog circuits on the same substrate as digital building blocks with a minimal overhead to the fabrication sequence. This implies using DG-MOSFETs with a minimal body thickness ($t_{\rm Si} \leq 30$ nm), oxide insulator thickness ($t_{\rm ox} \leq 5$ nm) and gate length ($L \leq 100$ nm), and the maximum $I_{\rm ON}/I_{\rm OFF}$ ratio optimized normally for minimum switching delaypower product [12]. It is also assumed that both gates have been optimized for a symmetrical threshold $V_T = \pm 0.25$ V using a dual-metal process. A generic DG-MOSFET structure based on these design guidelines and in agreement with experimentally demonstrated devices is given in Fig. 1(a). 2-D simulations of

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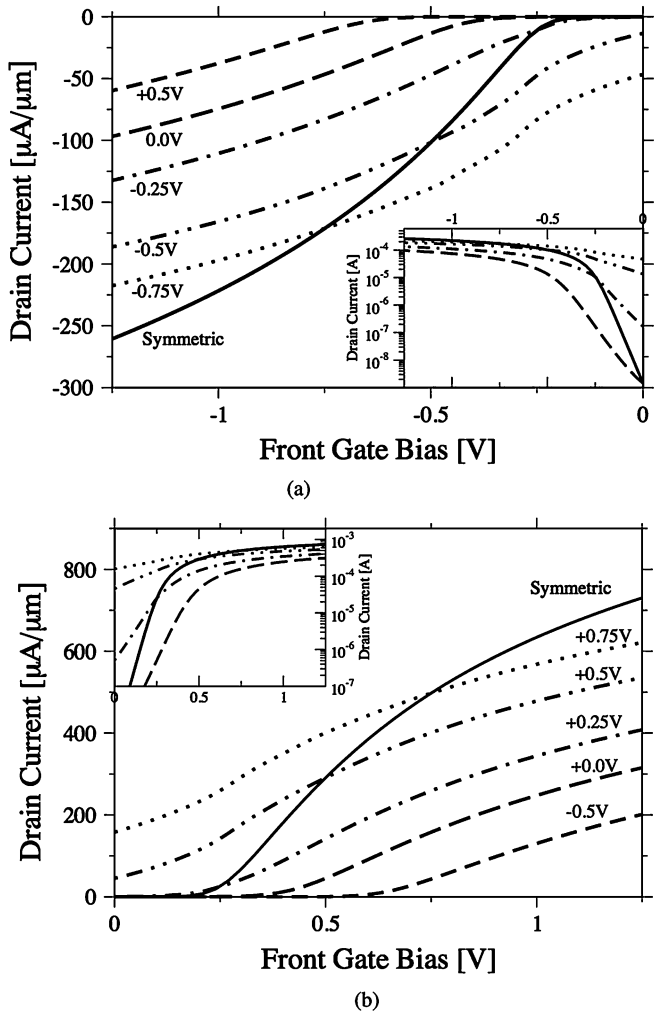

Fig. 2. Simulated characteristics of DG-MOSFETs used in this work. For both the (a) pMOSFET and (b) nMOSFETs, we provide $I_D - V_{\mathrm{Gtop}}$ plots for different back gate bias conditions labelled and $V_{\mathrm{DS}} = 1.0$ V. For comparison symmetric ($V_{\mathrm{bg}} = V_{\mathrm{fg}}$) drive is also included in the plots. Insets show the same data in semi-log scale, revealing the well-known degredation of subthreshold slope in asymmetrically driven DG-MOSFETs [14].

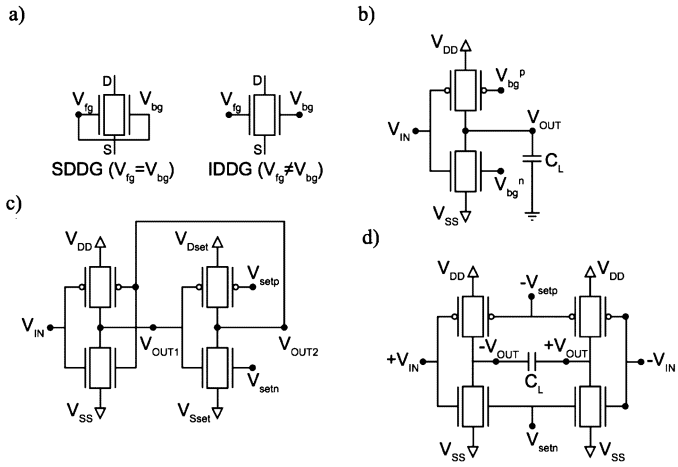

Fig. 3. (a) DG bias conventions SDDG and IDDG refer to *symmetrically* and *independently* driven double-gates, respectively. The main analog circuit blocks considered in this work incorporates (b) a simple CMOS analog amplifier, (c) a Schmitt trigger, and (d) an OTA-C integrator in which various IDDG configurations are employed to tune main performance metrics.

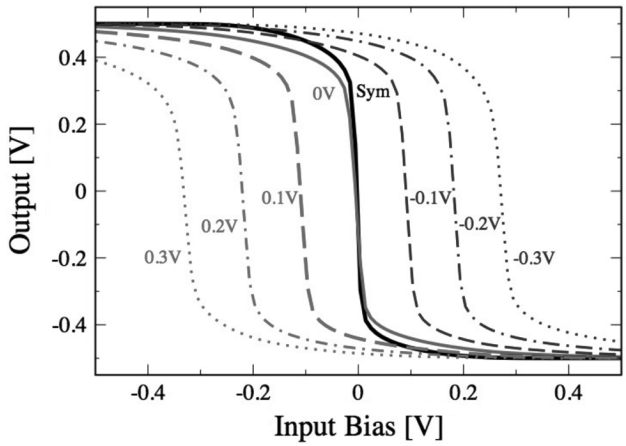

Fig. 4. Response of tunable DG-CMOS pair to setting the same voltage on the bottom gates ($V_{\mathrm{bg}}^{\mathrm{n}} = V_{\mathrm{bg}}^{\mathrm{p}}$). While the amplifier gain remains the same the amplification window shifts proportional to the applied control bias.

this structure are accomplished using DESSIS [13] in drift-diffusion approximation for carrier transport, which is sufficient for the low-power circuit-configurations explored here. Fig. 1(b) shows a typical current-density distribution in an asymmetrically biased n-type DG-MOSFET, where the higher bias of top-gate induces a more conductive channel.

With the device structure fixed, we can tailor its analog performance by the use of bottom-gate bias. This is best illustrated in Fig. 2(a) and (b), where the drain current through n- and p-type DG-MOSFETs driven from top-gate is studied as a function of the bottom gate bias. While the threshold of individual DG-MOSFETs can be modified using this approach, it must be pointed out that the resulting independently driven devices (IDDGs), [see Fig. 3(a)] are always inferior to symmetrically driven counterparts (SDDGs) in terms of transconductance and subthreshold performance, under equal geometry and bias conditions [14]. Thus, bottom-gate tunability comes with a reduction in intrinsic DG-MOSFET performance, a price well justified by the variety of circuit possibilities, as explored below. However, in terms of powerarea product, IDDG is superior over SDDG, and both of them over conventional devices, as recently discussed by Reddy *et al.* [7]

III. Simple CMOS Amplifier

The DG CMOS inverter pair [see Fig. 3(b)] constitutes one of the simplest yet most important design blocks also for analog circuit engineering. When biased in the transition region, it can serve as a high-gain push–pull amplifier. Depending on the selection of the sign and magnitude of the bottom-gate bias, the simple amplifier's characteristics can be altered in a number of ways, which greatly enhances the variety of applications for this otherwise simple circuit.

Fig. 4 shows that the setting of the CMOS pairs' bottom gates at the same voltage ($V_{\mathrm{bg}}^{\mathrm{n}} = V_{\mathrm{bg}}^{\mathrm{p}}$) results in proportional shifts in the voltage window for amplification. This "window shifting" can be conveniently utilized in a number of ways: in analog wave-shaping circuits sensitive to dc bias levels or in Schmitt triggers (see below). Please note that the amount of shift in this circuit is dictated by the strength of the capacitive coupling via the bottom-gate, which can be adjusted easily by the choice of

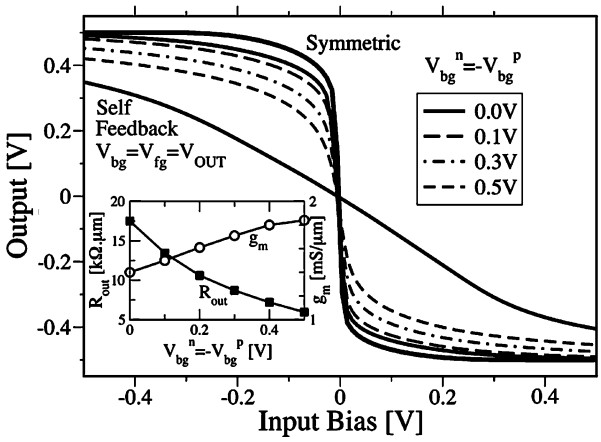

Fig. 5. Response of tunable DG-CMOS pair as a function of conjugate voltage on the bottom gates ($V_{\rm bg}^{\rm n} = -V_{\rm bg}^{\rm p}$). The amplifier gain changes with the applied control bias. The inset shows the change in the gain (g_m/g_d) is dominated by the output impedance ($R_{\rm out} = 1/g_d$) rather than the transconductance of the pair (g_m).

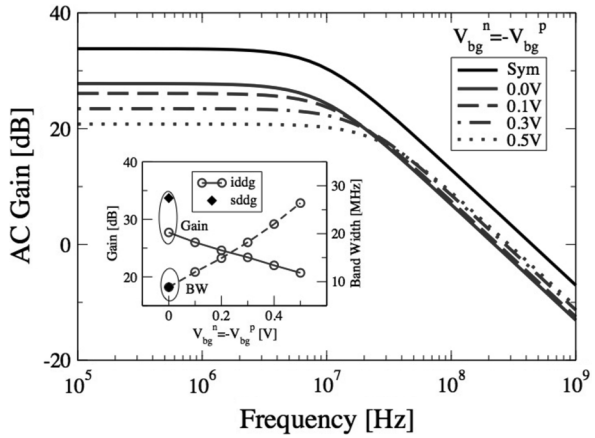

Fig. 6. AC analysis of DG CMOS amplifier driven with conjugate back-gate bias and loaded with $C_L = 1$ pF. The inset shows the gain-bandwidth tradeoff extracted from the main plot.

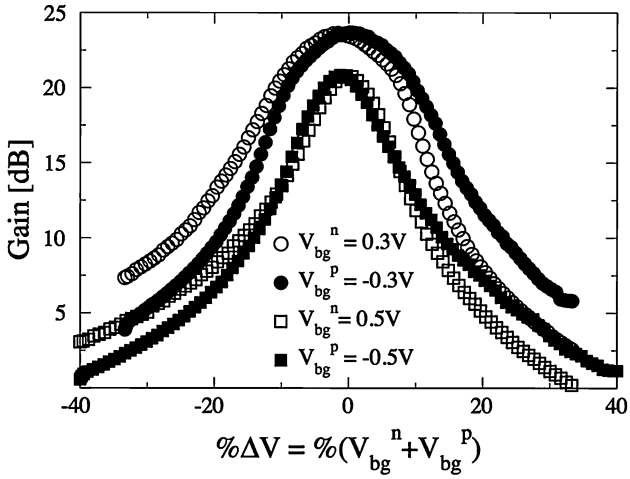

Fig. 7. Dependence of simulated ac gain on the conjugate biasing error, $\Delta; V = V_{\rm bg}^{\rm n} + V_{\rm bg}^{\rm p}$. In each case one of the back-bias points is held constant. For large errors (typically $\%\Delta V > 10$), such errors can lead to significant degredation of gain (> 3 dB). However, devices linearity suffers more from such errors as seen from resulting asymmetry of the curves.

gate insulator thickness, dielectric constant or the body thickness in a given technology.

An alternative scheme for programming the CMOS pair is conjugation, whereby the two complementary bottom-gates are driven by separate signals of equal magnitude but opposite polarity, i.e., $V_{\rm bg}^{\rm n} = -V_{\rm bg}^{\rm p}$. In a mixed-mode design using bipolar supply voltages, this biasing scheme is indeed possible and provides a method of varying the amplifier gain that may be highly desirable. As shown in Fig. 5, the slope (gain) of the transition region is a function of conjugate bias levels set on the bottom gates and the change in the output impedance (inset, $R_{\rm out} = 1/g_d$) dominates the simulated intrinsic gain (g_m/g_d) response. In principle, it should be possible to change the gain arbitrarily by application of an appropriate level of conjugate bias, whereas we have limited ourselves in Fig. 5 to ± 0.5 V, the bipolar supply voltages used in the low-power designs above.

For comparison, we also provide in Figs. 4 and 5 the output of SDDG CMOS pair. While the gain of this particular configuration is higher, without any bias control, it offers neither design latitude nor alternative configurations. Note that the output swing of IDDG amplifier is reduced as a result of back gate channel conducting even when the top channel is off, which can lead to higher static leakage. A similar problem occurs with the self-feedback arrangement included also in Fig. 5. In this case, the *output* of the IDDG CMOS pair drives their bottom-gates i.e., $V_{\rm bg}^{\rm n} = V_{\rm bg}^{\rm p} = V_{\rm OUT}$, which results in a very linear amplifier albeit with a significantly lower gain. This may be especially suitable in applications with stringent linearity requirements that cannot be served with other configurations or when a large signal buffer is required. It also provides a direct insight into the linearity-gain tradeoff not as well appreciated as the gain-bandwidth tradeoff in analog systems [15]. Such a gain-bandwidth tradeoff is readily illustrated in Fig. 6, which shows the outcome of ac analysis performed on the conjugate programming of the IDDG CMOS amplifier driving a load capacitor of $C_L = 1$ pF. The linear drop in the gain versus an increase in the bandwidth is well resolved in these simulations performed as a function of conjugate bottom-gate bias. The linear tuning response may be associated with the high-linearity of DG-MOSFETs [5] and its fully-depleted thin SOI body. The linearity of current MOSFETs is also visible in Fig. 2 as roughly equal spacing between back-bias steps above the respective thresholds for each device (approximately ± 0.25 V). Thus, it should be possible to fine tune simple CMOS amplifier's frequency response using the conjugate biasing scheme.

Errors ($\Delta V = V_{\rm bg}^{\rm n} + V_{\rm bg}^{\rm p}$) associated with conjugate biasing scheme can become a concern in practical implementations as a result of process variations and limited accuracy of the biasing networks. Fig. 7 provides a measure of this error for two example cases. Apparently, for large errors (typically $\%\Delta V > 10$), such bias imperfections can lead to significant degradation of gain (> 3 dB). However a more important consequence of this error is the poor linearity as a result of loss symmetry of the gain curves in Fig. 7. The asymmetry is the result of relative change in intrinsic gain of each transistor now operating under different conditions. Thus, in order to fully take advantage of tuning via conjugate biasing scheme, care is needed in its design and implementation.

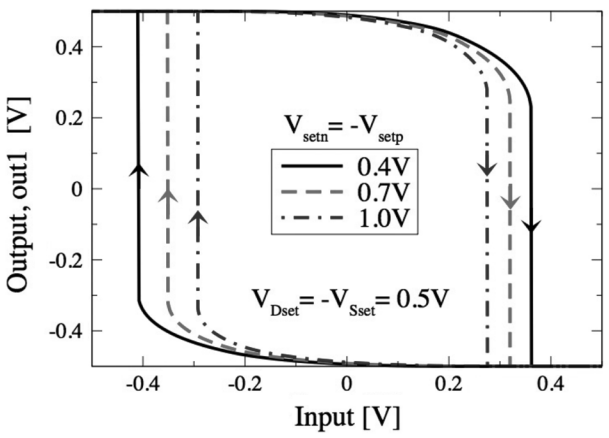

Fig. 8. Simulated dc response of a tunable *inverting* Schmitt Trigger built using only 4 DG-MOSFETs [Fig. 3(c)]. Note that large hystereses may be obtained with relatively small control voltages ($V_{\rm setn} = -V_{\rm setp}$) thanks to large gain of CMOS pair used in the second stage for feedback and the invertion is obtained at the output node *out1*.

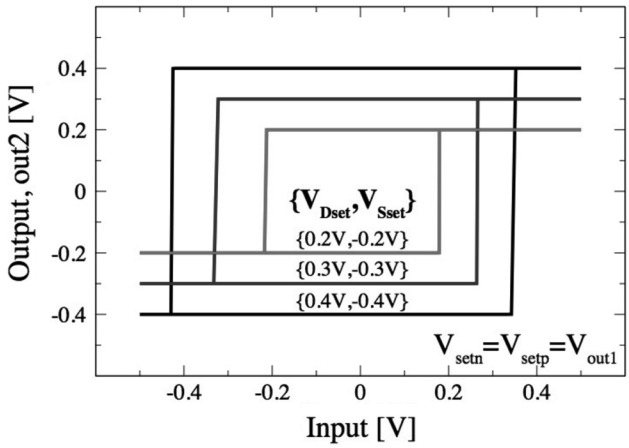

Fig. 9. Alternative design for a tunable noninverting Schmitt Trigger, where tunable rail voltages ($V_{\rm Sset}$ and $V_{\rm Dset}$) and a higher gain second stage with symmetric gates ($V_{\rm setn} = V_{\rm setp} = V_{\rm out1}$) are used. In this case the output is at node *out2*, thus noninverting, and the hysteresis can be scaled both vertically and horizontally using only 4 DG-MOSFETs.

IV. Schmitt Trigger

The ability to laterally shift the CMOS amplifier's transfer response paves the way for the construction of a simple Schmitt Trigger circuit, a nonlinear analog circuit block. The possibility of a DG Schmitt trigger is especially interesting for several reasons: i) leads to a reduction in both area and power [16] usage; ii) can also be used in static memory applications in digital circuits; iii) shows that significant leverage of device functionality is possible when feedback is included.

In our design, we use only four DG-MOSFETs as opposed to 6 MOSFETs needed in bulk CMOS design [16]. Previous attempts with DG-MOSFETs were either not tunable [16] or needed 6 transistors for tunability [17]. As indicated in Fig. 3(c), we consider a two-stage circuit with the conjugate programming of the second stage ($V_{\rm setp} = -V_{\rm setn}$) used to shift the first stage's response on the input plane to two opposite extremes. The simulated output of the Schmitt Trigger circuit is shown in Fig. 8, shown later, for three different bias settings. Note that between the up-sweep and down-sweep cases output makes transitions at different thresholds, as expected. The conjugate bias required to set the two extremes, i.e., the width of the hysteresis, can be decided from Fig. 4. Because of the relatively large gain of the second stage, very large hysteresis widths can be achieved. To design a small hysteresis, application of a relatively large conjugate bias may be needed, limiting the output swing of the second stage or the amount of shift for the first stage. An upper limit for the resulting power savings in this Schmitt Trigger circuit with four transistors is expected to be around 11% to 14%, as shown in [16].

It is also possible to scale the whole hysteresis by adopting a different topology in the second stage. In this case the rail voltages are the programming nodes ($V_{\rm Dset}$ and $V_{\rm Sset}$), and the back-gates are tied to front gates ($V_{\rm setp} = V_{\rm setn} = V_{\rm out2}$), i.e., the SDDG configuration of Fig. 3(a). The simulated characteristics of such a circuit are given in Fig. 9 for three rail voltage combinations. The hysteresis is scaled both vertically and horizontally, as the feedback voltage from the output of the second-stage changes. Also, the gain of the second stage is higher, resulting in *noninverting* hystereses with almost ideal shapes and more spacing between them.

Yet another way of optimizing the Schmitt Trigger circuits would be to reduce bottom-gate coupling by a thicker gate oxide, which would result in smaller shifts in Fig. 4 between bias settings. This requires process changes and may be a less desirable path than voltage tuning, which can be realized in a number of alternative fashions besides the above approaches. In any case, tuning via rail voltages may have its own limitations if the tuning circuitry cannot tolerate low-impedance nodes in the circuits above.

V. OTA

OTAs produce differential output currents in response to differential voltage inputs. They have become increasingly popular in the last two decades due to ease of design and reduction in circuit complexity compared to operational voltage amplifiers [18] in specific applications. They often drive a capacitive load in a compact OTA-C block that can act as very efficient integrators and appear also in other filter elements. Fig. 3(d) illustrates a simple OTA structure adapted from bulk MOSFET implementation, which normally requires six transistors [19], as opposed to 4 DG-MOSFETs used in Fig. 3(d). The availability of the individual bottom gates allows the elimination of the two extra transistors for transconductance (g_m) tuning across the two branches of the OTA, which saves both power and area.

Similar to the CMOS amplifier case, there are two tuning schemes available to this simple OTA circuit: an asymmetric bias ($V_{\rm setp} \neq V_{\rm setn}$) to shift frequency response or a conjugate bias ($V_{\rm setp} = -V_{\rm setn}$) to alter the transconductance (g_m) of OTA. Fig. 10 summarizes this latter case, where the frequency dependence of g_m on the conjugate programming voltage is plotted against frequency. The most important figure of merit g_m of OTA varies linearly with the programming voltage and the bandwidth of the OTA is constant despite varying g_m, which is one of the main hallmarks of OTAs [18]. The g_m is constant

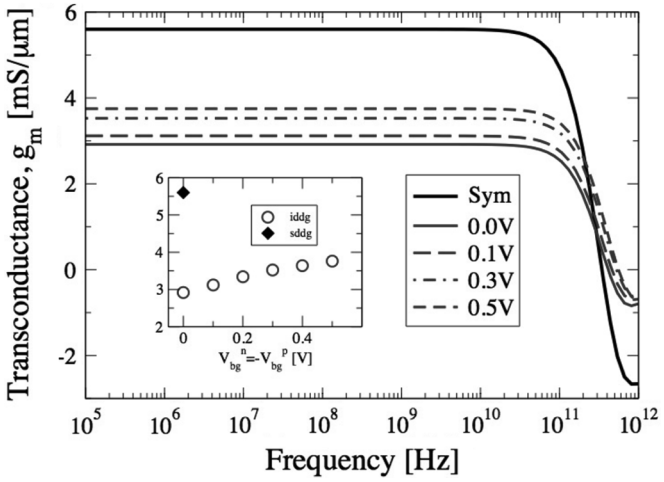

Fig. 10. Transconductance (g_m) of OTA circuit $(C_L = 0)$ in Fig. 3(d) versus frequency as a funtion of the conjugate tuning bias across the two CMOS pairs. g_m has a linear dependence (inset) on the bias setting and does not trade-off with the bandwidth as in the case of Fig. 6.

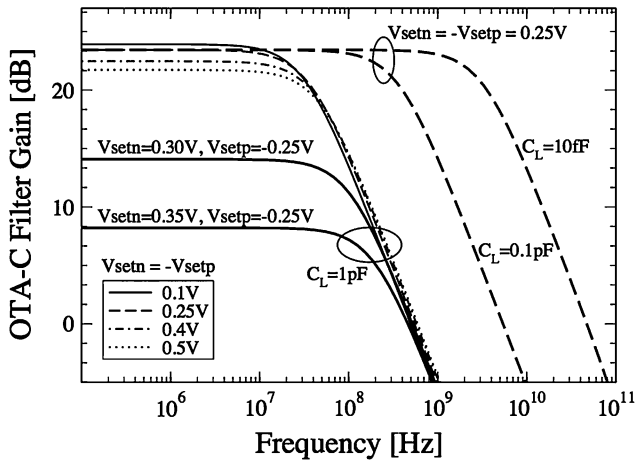

Fig. 11. AC gain of OTA-C filter of Fig. 3(d) at various bias settings and for three capacitance values. For a typical $C = 10$ fF, GHz operation is within reach. Although gain can be tuned using conjugate bias pairs, a wider tuning range is possible via assymetric bias $(V_{\rm setn} \neq -V_{\rm setp})$.

upto ∼100 gigahertz range limited by small parasitic capacitances on SOI substrate.

When an asymmetric bias is used to tune the OTA, we can conveniently shift the frequency response. For a fixed realistic load of $C_L = 10$ fF and $V_{\rm setn} = -V_{\rm setn} = 0.25$ V, the resulting OTA-C circuit serves as a low-pass filter with a corner frequency ~ 5 GHz, as shown in Fig. 11. Even for a relatively large load of $C_L = 1$ pF, the filter pass-band extends up to 200 MHz. The same corner frequency can be tuned almost a decade depending on the asymmetric bias on the back gates. This simple but powerful example aptly illustrates the potential of DG-MOSFET analog circuits in future mixed-signal nanosystems. More complicated examples of OTA with better common-mode rejection ratio, and other current-mode circuits, can also be built using DG-MOSFETs, which will be explored in a future work.

VI. Conclusion

Unique and novel examples of low-power analog circuit blocks based on DG-MOSFETs have been investigated. Using mixed-mode (device+circuit) TCAD simulations, we have shown how the bottom-gate of an independently driven DG-MOSFETs may be used to design and test analog circuits with tunable performance metrics. In particular, we have provided examples for a simple CMOS amplifier pair, a Schmitt Trigger circuit and an OTA-C filter. In all cases, the main figures of merit, the gain, the hysteresis and the transconductance, respectively, can be varied by application of a specific bottom-gate bias conditions that provide local changes in CMOS pair response. In particular, it has been identified that a single (identical) or a conjugate (i.e., opposite in sign) biasing of n- and p-type devices are preferable for most cases, resulting in a wide tuning range of performance figures, provided that voltage tuning can be established with good $(< 10\%)$ accuracy. The circuits and biasing schemes explored here show how the nanoscale DG-MOSFETs may pave way for efficient, tolerant and smaller circuits with tunable characteristics.

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