A DC–DC Charge Pump Design Based on Voltage Doublers

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***Abstract*—A novel organization of switched capacitor charge pump circuits based on voltage doubler structures is presented in this paper. Each voltage doubler takes a dc input and outputs a doubled dc voltage. By cascading n voltage doublers the output voltage increases up to 2^n times. A two-phase voltage doubler and a multiphase voltage doubler (MPVD) structures are discussed and design considerations are presented. A simulator working in the Q–V realm was used for simplified circuit level simulation. In order to evaluate the power delivered by a charge pump, a resistive load is attached to the output of the charge pump and an equivalent capacitance is evaluated. A comparison of the voltage doubler circuits with Dickson charge pump and Makowski's voltage multiplier is presented in terms of the area requirements, the voltage gain, and the power level. This paper also identifies optimum loading conditions for different configurations of the charge pumps. Design guidelines for the desired voltage and power levels are discussed. A two-stage MPVD was fabricated using MOSIS 2.0-μm CMOS technology. It was designed with internal frequency regulation to reduce power consumption under no load condition.**

I. Introduction

A CHARGE pump circuit provides a voltage that is higher than the voltage of the power supply or a voltage of reverse polarity. In many applications such as the Power IC, continuous time filters, EEPROMs, and switched-capacitor transformers, voltages higher than the power supplies are frequently required. Increased voltage levels are obtained in a charge pump as a result of transferring charges to a capacitive load, and do not involve amplifiers or regular transformers. For this reason, a charge pump is a device of choice in semiconductor technology where the normal range of operating voltages is limited. Charge pumps usually operate at a high- frequency level in order to increase their output power within a reasonable size of total capacitance used for charge transfer. This operating frequency may be adjusted by compensating for changes in the power requirements and saving the energy delivered to the charge pump.

Among many approaches to the charge pump design, the switched-capacitor circuits such as Dickson charge pump [1] are very popular, because they can be implemented on the same chip together with other components of an integrated system. An extensive research focused on the design and timing scheme of Dickson charge pump such as [2]–[5]had been accomplished. Witters *et al.* [2] provided a detailed analysis of Dickson multiplier built in very large scale integration (VLSI) technology with diodes realized by nMOS transistors. They considered the effects of the threshold voltage and the leakage current, as well as conducted a number of experimental measurements. Cataldo and Palumbo [3] presented an optimized design methodology for double and triple charge pumps, and in [4] they discussed a dynamic model of an n-stage Dickson charge pump useful for a pencil and paper design. In [5] Tanzawa and Tanaka provided a detailed dynamic analysis of the Dickson pump and derived analytical expressions for the rise time and current consumption. They also estimated boosting energy and the optimum number of stages to minimize the rise time. The voltage gain of the Dickson charge pump is proportional to the number of stages in the pump. It may require quite a many devices and a silicon area, when a charge pump with the voltage gain larger than 10 or 20 is needed. Such high voltage gains are required for low voltage EEPROMs, and typically more than three stages of Dickson charge pump are used. Improved Dickson charge pumps for low voltage EEPROMs and flash memories were developed and discussed in [6]–[8]. Authors in [6] proposed the negative gate biased source erase scheme and supporting circuitry. The pulse timing was adjusted to maintain high efficiency of energy transfer. For a large voltage gain, Makowski [9] introduced an n stages charge pump with its final voltage gain limited by $(n+1)$th Fibonacci number. Researchers have focused on different issues related to practical implementation of the charge pump starting from its topological properties [9], voltage gain, and dynamic properties [5] to improvements in efficiency and power considerations [10].

The charge pump operates by charging and discharging capacitances, transferring energy to the output load. By reducing switching frequency, whenever a requirement for the load current is low, the switching energy is saved and pump efficiency is improved, as discussed in [10]. In addition, simulation and measurement results presented in [10] indicated a strong dependence of the output voltage on the load resistance. There is a need for better understanding of the design tradeoffs related to charge pump design.

This paper focuses on switched-capacitor charge pumps that have exponentially growing voltage gain as a function of the number of stages. This kind of charge pumps described first in [11], are constructed by several cascaded voltage doublers, with n cascaded voltage doublers providing the voltage gain of up to 2^n. Voltage doublers are analyzed in Section II, where the topological method introduced by Makowski is used to evaluate their voltage gain. Design considerations of the voltage doublers are presented in Section III were tradeoffs between

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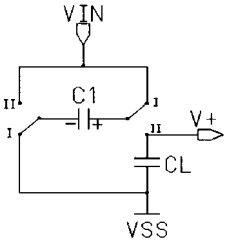

Fig. 1. Voltage doubler.

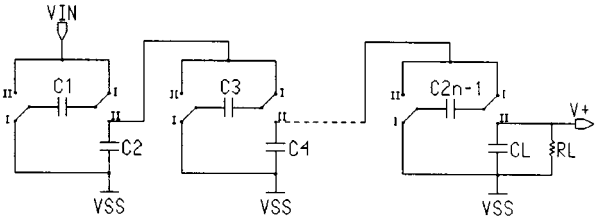

Fig. 2. TPVDs (simply cascaded).

power, frequency, and voltage level are addressed. Recommendations for the optimum loading conditions are expressed as a function of output power and voltage levels. Section IV discusses power, timing and frequency issues in a limited design area. A two-stage voltage doubler with frequency regulation was designed, fabricated, and tested using MOS technology as discussed in Section V. Section VI presents the conclusion.

II. Voltage Doublers

A switched-capacitor organization of a two-phase voltage doubler (TPVD) is shown in Fig. 1. VIN is the power supply, and $V+$ is the voltage output. For a simple explanation of its operation, let us assume that the voltage doubler starts in phase I (as shown in Fig. 1). Capacitor C1 is charged to the input voltage VIN, and CL is assumed to have no initial charge. In phase II, the lower voltage terminal of C1 is connected to the power supply and its upper terminal is connected to CL. The charge stored in C1 is shared with CL, and the final output voltage $V+$ is equal to VIN plus a voltage due to the final charge in the capacitor C1. The charge sharing allows $V+$ to grow. Subsequently, when the voltage doubler goes back to phase I, C1 is recharged to VIN, and CL keeps the previous charge. Then, the circuit is switched to phase II again. Final output voltage value is greater than the previous one due to the additional charge stored in CL. By repeating these operations many times, the output voltage keeps growing to the final voltage 2*VIN. To achieve a voltage gain higher than 2, we can cascade the voltage doublers as shown in Fig. 2. The output voltage of previous voltage doubler is the power supply of the next voltage doubler.

In his study of switched-capacitor voltage multiplier circuits [9], Makowski established a theoretical limit on the voltage gain in a two-phase multiplier and related it to Fibonacci numbers. Makowski proposed a new organization of two-phase charge pump as shown in Fig. 3. An n-stage Makowski charge pump needs $2n$ capacitors and $3n-1$ switches and has a voltage gain equal to the $2n$th Fibonacci number which is higher than the voltage gain of simply cascaded voltage doublers. While the

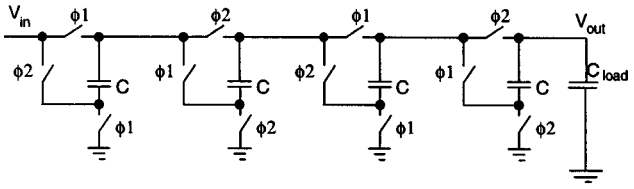

Fig. 3. Makowski charge pump.

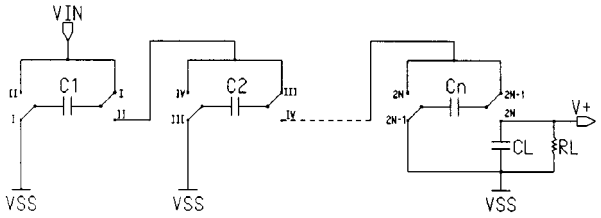

Fig. 4. MPVD.

voltage doubler presented in Fig. 2 does not provide a maximum theoretical voltage gain determined by the upper bounds set by Makowski's work, it yields a regular and efficient structure with the output voltage level compatible with a binary system.

The following conjecture sets the voltage gain limit for the multiphase voltage doublers (MPVDs).

Conjecture: The realizable conversion ratio of a multiphase dc–dc switched-capacitor voltage multiplier with a single voltage source without transformers is limited by

$$M(n) = \frac{V_{\text{out}}}{V_{\text{in}}} = 2^n \tag{1}$$

where

- $M(n)$ maximum voltage gain for the multiplier with n capacitances;
- V_{out} output dc voltage;
- V_{in} input (source) dc voltage.

Oota *et al.* [11] proposed a multiphase charge pump that has a voltage gain 2^n using $n+1$ capacitors and $3n+1$ switches. It requires $2n$ clock signals to control these switches. In this paper, we consider a modified organization of the multiphase charge pump as shown in Fig. 4. This circuit includes four switches per a single capacitor, which is larger than the number of switches per capacitor $(3+1/n)$ in the Oota's voltage multiplier. However, MOS switches designed in the charge pumps use a much smaller area than capacitors, and have a limited effect on the pump performance. The voltage doubler shown in Fig. 4 has a simpler clock organization than [11], and its clock signals can be generated by the frequency division.

Fig. 5 shows eight different states of a three-stage charge pump based on the MPVDs that attains the voltage gain of 8. At the output of this charge pump, the load capacitor C_{load} is used to accumulate the charge. If the voltage-controlled switches are used to implement this charge pump, three different frequencies of clocked signals are required. Because the circuit in Fig. 2 works with the two-phase clock we call this structure a TPVD in differentiation to the circuit presented in Fig. 4 which is identified as an MPVD.

To compare various charge pumps, we chose circuits with the voltage gain $A_V = 8$ for which the voltage doublers require

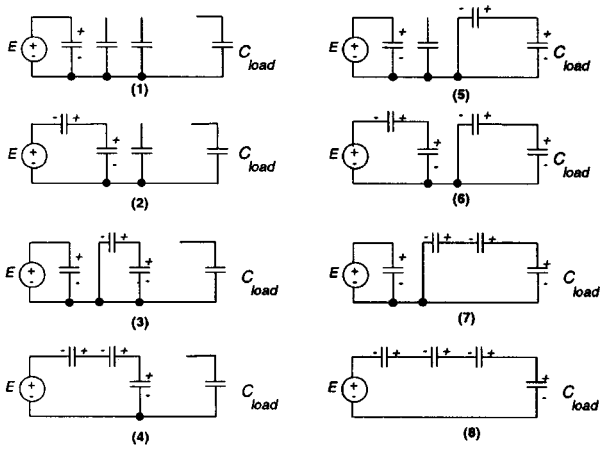

Fig. 5. A three-stage charge pump based on MPVDs .

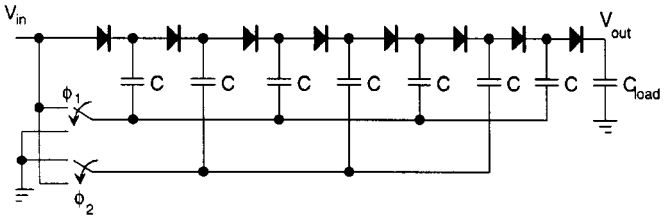

Fig. 6. Dickson charge pump.

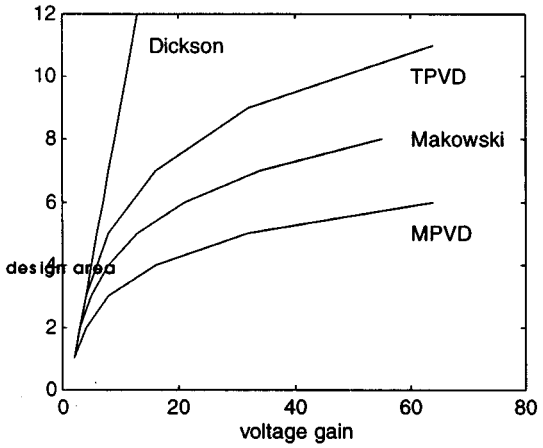

Fig. 7. Number of capacitors as a function of the voltage gain.

3 stages, Dickson charge pump (Fig. 6) requires eight stages, and Makowski charge pump requires four stages. Dickson charge pump exhibits a linear growth of the number of devices used with the voltage gain level, while the voltage doublers and Makowski charge pumps requirements for the devices grow logarithmically with the voltage gain (Fig. 7). Table I shows the required number of devices for constructing charge pumps with the voltage gain equal to 8.

To observe the behavior of n-stage charge pumps the computer simulation program SAMOC based on Q–V realm analysis was used [12]. This program generates the charge conservation equations at capacitive nodes, and uses modified nodal-like equations for independent and voltage controlled voltage sources, ideal switches, and ideal diodes. The Q–V realm analysis is accomplished by solving the charge conservation equations

$$\boldsymbol{C}\boldsymbol{V} = \boldsymbol{Q} \tag{2}$$

where

$\boldsymbol{C}$ modified nodal capacitance matrix;
$\boldsymbol{V}$ voltage vector;
$\boldsymbol{Q}$ initial charge vector.

Related to the number of capacitors used in a charge pump, is the energy needed to drive the pump to a desired voltage level. Since the energy stored in a capacitor is proportional to the product of the capacitance value, and square of the voltage across the capacitance, we can estimate the total energy delivered to an $(N-1)$-stage $(A_v = N)$ Dickson charge pump including the energy stored in the load resistor C_{load} using

$$\begin{aligned} W_D &= \sum_{i=1}^{N-1} \tfrac{1}{2} C[V(i)]^2 + \tfrac{1}{2} C_{\text{load}}(NV_{\text{in}})^2 \\ &= \sum_{i=1}^{N} \frac{1}{2} C(iV_{\text{in}})^2 = \frac{N(N+1)(N+2)}{12} CV_{\text{in}}^2 \end{aligned} \tag{3}$$

where in order to simplify discussion we assumed that $C = C_{\text{load}}$. By comparison, the total energy delivered to an M-stage TPVD charge pump with the same voltage gain $(A_v = N)$ can be estimated from

$$\begin{aligned} W_{vd1} &= \sum_{i=1}^{M} \tfrac{1}{2}(C_{2i-1}V_{C_{2i-1}}^2 + C_{2i}V_{C_{2i}}^2) \\ &= \sum_{i=1}^{M} \frac{C}{2}[(2^iV_{\text{in}})^2 + (2^{i-1}V_{\text{in}})^2] = \frac{5(N^2-1)}{6} CV_{\text{in}}^2 \end{aligned} \tag{4}$$

while assuming $C_{2i} = C_{2i-1} = C$. For the MPVD charge pump with the same voltage gain the delivered energy can estimated by

$$\begin{aligned} W_{vd2} &= \sum_{i=1}^{M} \tfrac{1}{2}[CV_i^2 + C_{\text{load}}V_{\text{out}}^2] \\ &= \frac{C}{2} \sum_{i=0}^{M} (2^iV_{\text{in}})^2 = \frac{(4N^2-1)}{6} CV_{\text{in}}^2 \end{aligned} \tag{5}$$

while $C_{\text{load}} = C$ and the number of stages $M = \log_2(N)$. In the above equations, we considered all capacitances of equal values. As we can see from the obtained results the boosting energy increases quadraticly with the voltage gain in the TPVD charge pump as opposed to the cubic increase in the Dickson charge pump. Fig. 8 shows the boosting energy as a function of the voltage gain for these three charge pumps. The Dickson charge pump requires much more boosting energy than voltage doublers for the high voltage gains.

Voltage doublers can be built either as switched capacitor transformers with discrete components (useful in power electronics) as described in [11], or be integrated on an IC chip. In the first case large output power and large voltages require power MOSFETs and large discrete capacitors, while in the

TABLE I
REQUIRED NUMBER OF DEVICES FOR CHARGE PUMPS WITH VOLTAGE GAIN $A_V = 8$

	TPVD	Dickson	Makowski	MPVD
***n* (number of stages)**	3	7	4	3
switches	12	0	12	12
Floating capacitors	3	7	4	3
Grounded capacitors	2	0	0	0
diodes	0	8	0	0

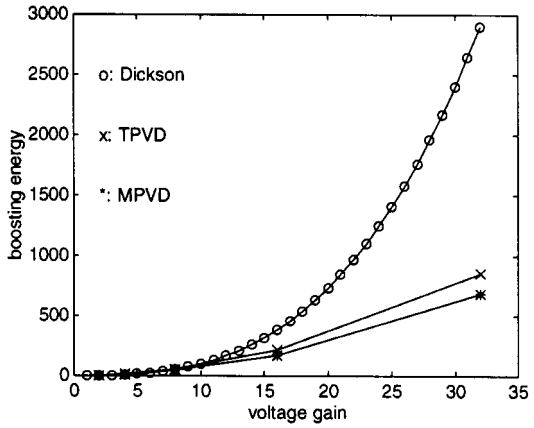

Fig. 8. Boosting energy as a function of voltage gain for Dickson, TPVD and MPVD charge pumps.

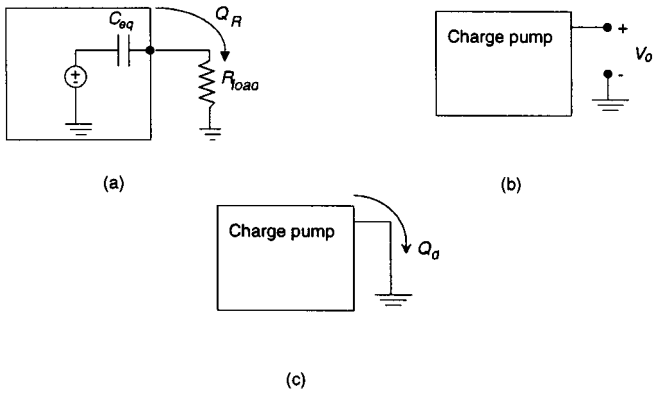

Fig. 9. The evaluation of the equivalent capacitance network.

second case smaller power (and output voltage) can be delivered by small capacitors operating at higher frequencies. The design considerations are different for these two basic types of applications. This study helps to understand voltage doublers and their design tradeoffs.

III. OPTIMIZED POWER TRANSFER CONSIDERATIONS

The charge pump circuit analysis and the simulation results presented so far are obtained under the assumption that there is no power loss in the charge pump circuits, and that the electric charge transfer is instantaneous. After the output of such a charge, the pump reaches its maximum voltage level, there will be no energy driven from the supply source. In the real world application, charge pumps will drive electronic devices that can be treated as resistive loads. A simple way to estimate the effect of the resistive load on the operation of a charge pump is to solve the output circuit equation considering the output resistance R_{load} and the equivalent charge pump circuit [shown in Fig. 9(a)]. By estimating the equivalent capacitance C_{eq}, the electric charge dissipated by the load resistor R_{load} during a clock period can be evaluated from

$$Q_R = V_o C_{\text{eq}} \left(1 - \exp\left(-\frac{T}{R_{\text{load}} C_{\text{eq}}}\right)\right) \tag{6}$$

where V_o is the output voltage when R_{load} is absent [Fig. 9(b)], and T is the clock period. After evaluating Q_R, we can modify the Q–V realm equations as follows:

$$\boldsymbol{CV} = \boldsymbol{Q} - Q_R \boldsymbol{d} \tag{7}$$

where $\boldsymbol{d}$ is the selection vector, $V_{\text{out}} = \boldsymbol{d}^t \boldsymbol{V} = V_R$. That is, the load resistor in the Q–V realm analysis is treated as a voltage dependent charge drain that removes electric charge from the equivalent capacitance C_{eq}. The equivalent capacitance C_{eq} is estimated by putting a dummy voltage source $V_d = 0$ V in the output [see Fig. 9(c)]. The electric charge Q_d, goes through the dummy voltage source and can be obtained from simulation of the shorted charge pump formulating the modified nodal-like equations. Then, the equivalent capacitance C_{eq} can be estimated using

$$C_{\text{eq}} = \frac{Q_d}{V_o} \tag{8}$$

where V_o is the open circuit output voltage used in (6). The resistive load analysis requires 2 Q–V realm analyses in each clock phase instance. The first one is to evaluate the equivalent capacitance C_{eq}, and the second one is to calculate the effect caused by removing Q_R from the output of the charge pump (6).

In order to illustrate the effect of the resistive load on the output voltage and the amount of the output power delivered, a TPVD charge pump with four cascaded voltage doublers was used with different values of the load resistance, R_{load}. The pump capacitors are 100 pF, and the clock period T is 40 ns with power supply 5 V. The load resistances used were 2 kΩ, 20 kΩ, 200 kΩ, and infinity. Fig. 10 shows the simulation results for the first 1500 iterations. In the plot, we can find out that the charge pump can no longer supply the 16× output, while the R_{load} is present. The load resistor R_{load} drains the electric charge supplied by the charge pump and the output voltage decreases.

The resistive load analysis can be used to estimate the output power of a charge pump for different values of R_{load} and output voltages. To obtain the power and output voltage characteristics of a charge pump, R_{load} values from 100 Ω to 1 MΩ were used in simulation. The power delivered by the charge pump P_R as a function of R_{load} is plotted in Fig. 11. Based on the results of

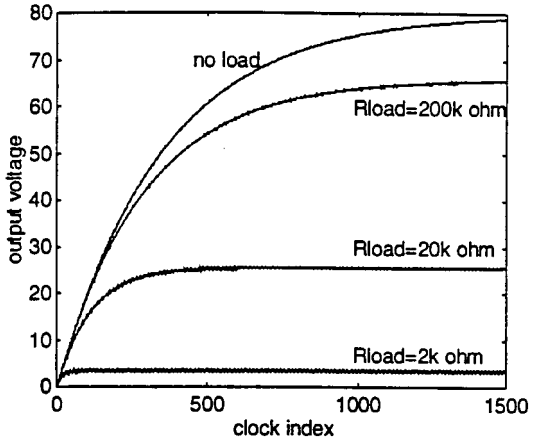

Fig. 10. The 4-stage TPVD charge pump output voltage with different values of $R_{\rm load}$.

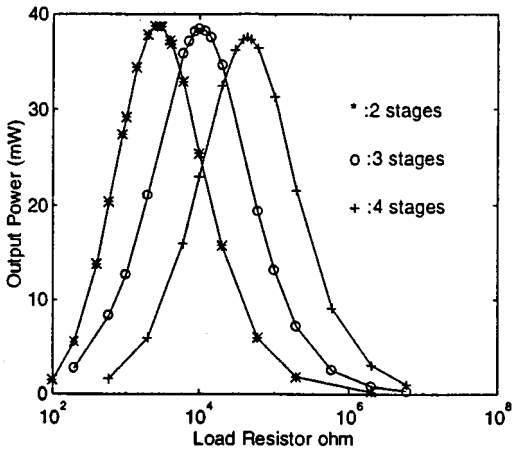

Fig. 11. The output power as a function $R_{\rm load}$ for TPVD charge pumps with different number of stages.

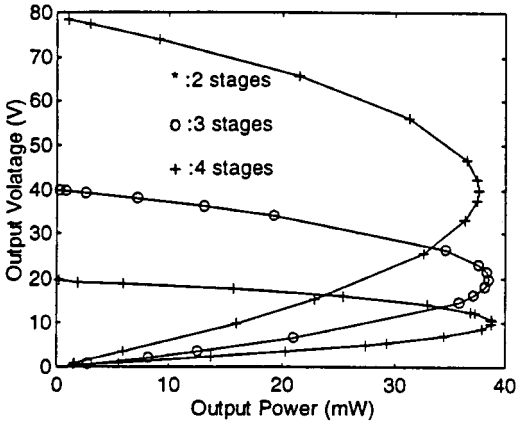

Fig. 12. Output voltage as a function of output power for TPVD with different number of stages.

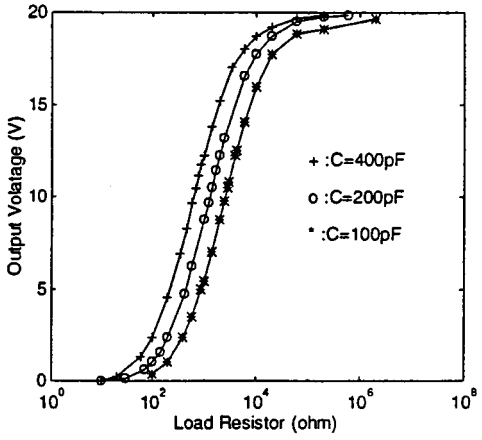

Fig. 13. Output voltage of 2-stage TPVD as a function of load resistance and pump capacitance.

charge pump analysis we can formulate the following conjecture.

Conjecture: Increasing the number of voltage doublers does not have a strong effect on the maximum output power delivered by the charge pump. This power is a function of the energy transport efficiency and depends mainly on the capacitance sizes and the clock frequency.

Fig. 12 shows V_R as a function of the output power P_R. Based on the simulation results another conjecture can be formulated.

Conjecture: A charge pump delivers its maximum output power at a specific value of $R_{\rm load}$, and at this optimum load, the output voltage drops to one half of its maximum value measured on the open circuit output terminals.

Alternatively, we could represent the load as a required current and find relationship between the output current and the power delivered to the output load. This relation is similar to the power voltage relation shown in Fig. 12, however, the characteristics do not depend on the number of stages.

Simulation of the TPVD charge pump with two voltage doublers shows a maximum output power equal to 38.8 mW for the load resistance $R_{\rm load} = 3$ kΩ and all the capacitors in the charge pump equal to 100 pF. The TPVD charge pump with three voltage doublers has the maximum output power equal to 38.5 mW for $R_{\rm load} = 10$ kΩ, and the charge pump with four voltage doublers has a maximum output power equal to 37.6 mW, for $R_{\rm load} = 42.4$ kΩ. It is obvious that the growth of the optimum output power is linear with the capacitance size. In addition, as we can observe from Fig. 13, the output voltage is smaller when the load resistance is reduced and it remains unchanged when the product of load resistance and capacitance is constant. This result combined with the evaluated optimum load resistances can be used to determine the optimum load resistance for any size of the pump capacitance. For instance, if capacitances of the three-stages TPVD pump were increased ten times, then the optimum load resistance will be 1 kΩ, and the pump will deliver 385 mW of the output power.

Since the optimum power is obtained at the same voltage level for a given charge pump, we can find dependence between the output power level and the optimum load resistance using

$$P_o = \frac{V_{\rm out}^2}{R_{\rm load}} = K\ f\ C \qquad \Rightarrow \quad R_{\rm load} = \frac{V_{\rm out}^2}{K\ f\ C} \tag{9}$$

where K is a constant for a given charge pump organization and is independent on the number of stages (in the TPVD design $K \sim 15.4V^2$). This indicates that the optimum load resistor is in inverse proportion to the values of the charge pump capacitance used. For instance, if the charge pump with two voltage doublers uses 100 pF capacitors and clock frequency is 40 MHz, then the

maximum power transferred to the load will be 38.5 mW and the optimum load resistance can be estimated as

$$R_{\text{load}} = \frac{V_{out}^2}{K\ f\ C} = \frac{(20/2)^2 v^2}{38.5\ \text{mW}} = 2.6\ \text{k}\Omega. \tag{10}$$

Equation (9) can also be used to evaluate the charge pump capacitance needed to deliver specified amount of power to a given load. Finally, based on (9) we can see that the optimum load of a voltage doubler is proportional to the square of its output voltage.

Design considerations have to include different aspects of delivering a maximum amount of power at the desired voltage level by a circuit that occupies the least area and can be easily integrated with other digital devices on the same chip. From the conducted study, it is clear that we can trade the power for the area in designing a charge pump. The larger the area for a given voltage, the larger the output power.

IV. Power, Timing and Frequency Considerations

Modern IC fabrication technology requires realization of the designs with a minimum area and energy dissipation. It was demonstrated in Section II that the boosting energy requirements of a similarly sized Dickson charge pump is higher than that of the voltage doublers or Makowski charge pumps. This result was obtained under the assumption of equal size capacitances in all pumps, which may be considered in a discrete design with large capacitors. If capacitance sizes are adjusted to fit a specified design area then (3)–(5) will change.

First, let us analyze the voltage gain efficiency of various designs at a restricted amount of silicon area. Let us assume that each charge pump uses capacitors of the same sizes. Assume also that the design area A is divided into equal size capacitances and that there is no overhead for designing switches and diodes. The following shows dependence of the capacitor sizes on the voltage gain in different designs:

$$C_D \approx \frac{A}{A_v} \tag{11}$$

in Dickson charge pump

$$C_{vd} \approx \frac{A}{\alpha \log_2 A_v} \text{ where } \alpha = \begin{cases} 2, \text{ for TPVD} \\ 1, \text{ for MPVD} \end{cases} \tag{12}$$

in the voltage doublers

$$C_M \approx \frac{A}{F^{-1}(A_v)} \tag{13}$$

in the Makowski charge pump, where $F^{-1}(A_v)$ is the inverse of the Fibonacci function for a given voltage gain.

Applying (11)–(13) to the estimates of boosting energy (3)–(5) in different charge pumps, we can directly express the boosting energy as a function of the voltage gain $V\text{out}/V\text{in} = N$. The following results show that in a Dickson charge pump

$$W_D = \frac{N(N+1)(N+2)}{12} C V_{\text{in}}^2 = \frac{N(N+1)(N+2)}{12}\ \frac{A}{N} V_{\text{in}}^2 = \frac{(N+1)(N+2)}{12} A V_{\text{in}}^2 \tag{14}$$

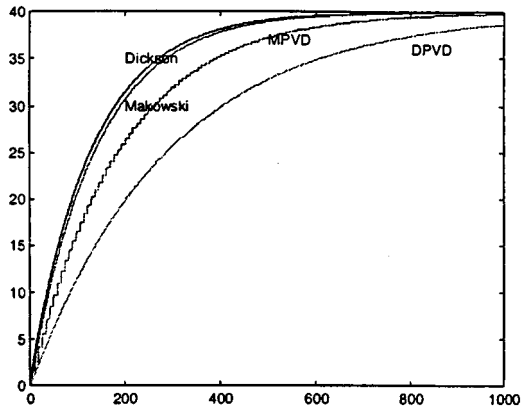

Fig. 14. Comparison of the boosting time using constant design area.

the boosting energy increases quadraticly with the voltage gain. In the TPVD's, the boosting energy is

$$W_{vd1} = \frac{5(N^2-1)}{6} C V_{\text{in}}^2 = \frac{5(N^2-1)}{6}\ \frac{A}{2\log_2 N} V_{\text{in}}^2 = \frac{5(N^2-1)A}{12\log_2 N} V_{\text{in}}^2 \tag{15a}$$

and in the MPVDs

$$W_{vd2} = \frac{4N^2-1}{6} C V_{\text{in}}^2 = \frac{4N^2-1}{6}\ \frac{A}{\log_2 N} V_{\text{in}}^2 = \frac{(4N^2-1)A}{6\log_2 N} V_{\text{in}}^2 \tag{15b}$$

so the boosting energy of voltage doublers increases less than quadraticly with the voltage gain.

Different charge pumps have different output driving ability. For instance Fig. 14 shows comparison of the boosting time for voltage gain of 8 in different structures under constant design area.

An important issue to consider in a practical design of a charge pump is the minimization of boosting time. In their study of dynamic charge pump analysis [5], Tanzawa and Tanaka indicated that in order to optimize the design for the minimum rise time a number of stages in the charge pump has to be increased. They established that for the Dickson charge pump, the optimum increase is 1.4 times the minimum number of stages required for a given voltage gain. This optimization was reached under the assumption of constant design area and a fixed load capacitance. With the increased number of stages, the output voltage can be larger. On the other hand, smaller capacitances take longer to deliver enough charges to rise the output voltage to the specific level.

One method to find out the shortest boosting time for a specified desired voltage value under a constant design area is to do timing simulations of different number of stages under this design constrain. The higher the desired boosted voltage value, the larger the number of stages the designed charge pump should have. For example, if a voltage gain of 20 is required, the TPVD or MPVD charge pump should contain at least five voltage doublers. On the other hand, the more the voltage doublers used, the

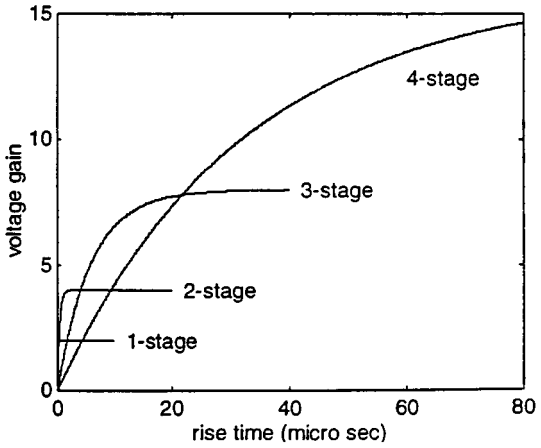

Fig. 15. Rise time optimization of TPVD charge pump.

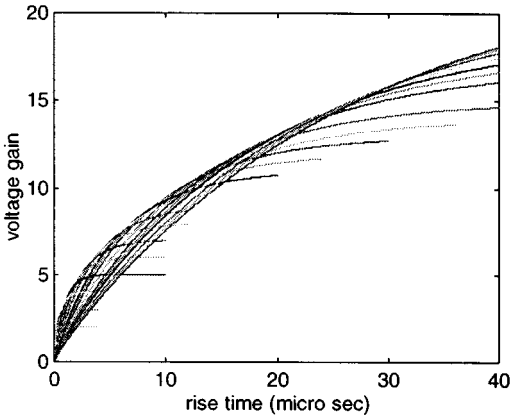

Fig. 16. Rise time optimization of fixed area design Dickson charge pump.

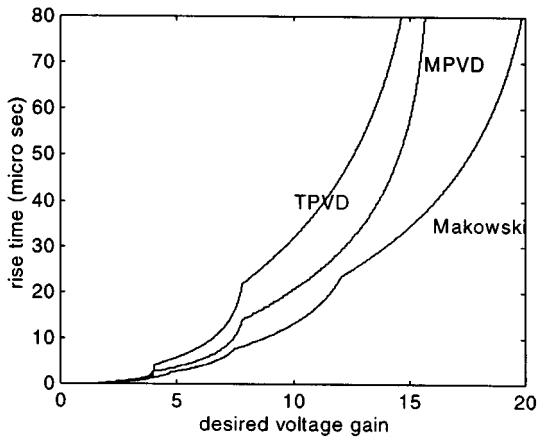

Fig. 17. Optimized boosting time as a function of desired voltage.

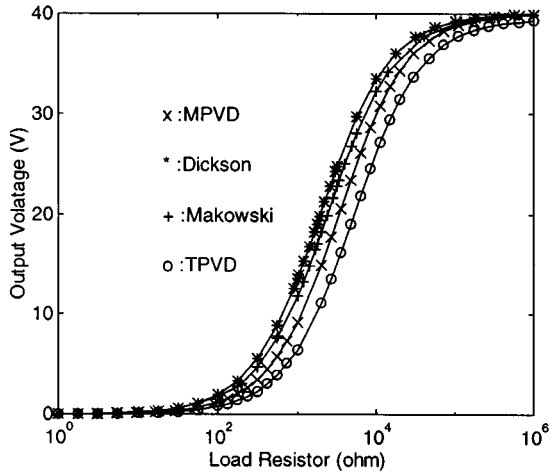

Fig. 18. Fixed area design: output voltage as a function of the load resistance.

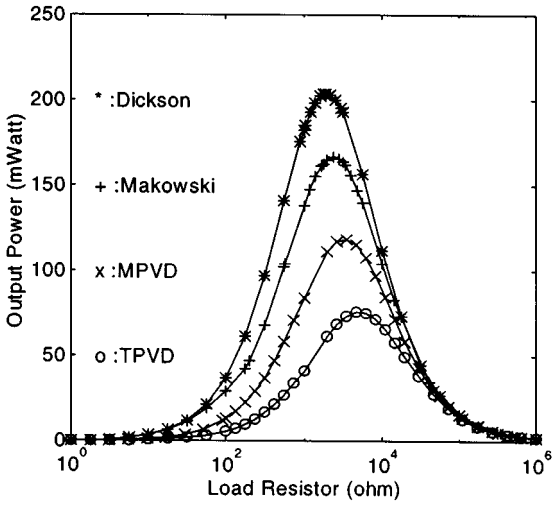

Fig. 19. Fixed area design: output power as a function of the load resistance.

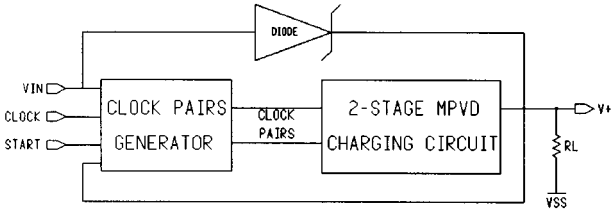

Fig. 20. Diagram of 2-stage MPVD.

larger the number of capacitors is required. For constant area design, larger number of capacitors means smaller size of each capacitor in the designed charge pump and less power delivered to a load capacitor. Fig. 15 shows the timing analysis of 1-stage, 2-stage, 3-stage and 4-stage TPVD charge pumps, the design area is 1 nF and the load capacitor is also 1 nF. By choosing the upper bound of all curves we can determine the pump size (maximum voltage gain) for which a desired output voltage is reached in the minimum time. By using similar analysis of Dickson charge pumps we could confirm the optimum relation established in [5] that specifies the number of stages required for reaching a desired voltage level in a minimum boosting time. The simulation results, which confirm findings of optimum charge pump size, is shown in Fig. 16. If we invert the voltage-time relationship to a time-voltage relationship, then, an optimized boosting time is obtained as a function of desired output voltage. Fig. 17 shows the optimized boosting time as a functions of the output voltage for TPVD, MPVD and Makowski charge pumps.

If a constant design area is used, power transfer ability of the voltage doublers as well as the Makowski charge pump improves in relation to the Dickson charge pump. Figs. 18 and 19 show the output voltage and power delivered by different charge pumps as a function of the load resistance for voltage gain of 8,

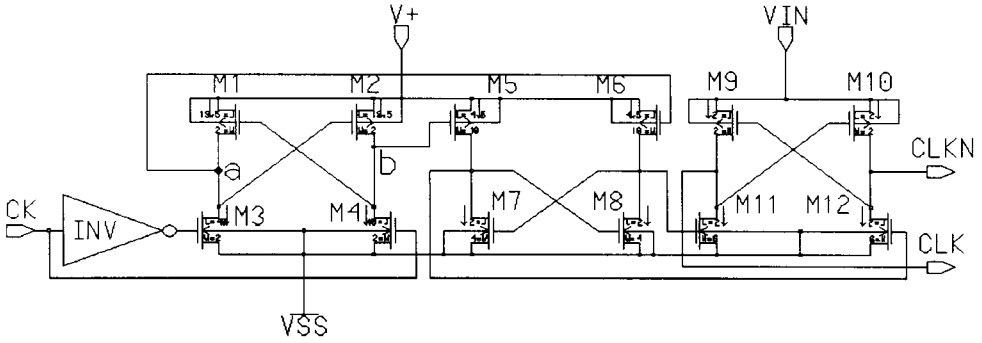

Fig. 21. Frequency regulator.

under the assumption of a constant design area. The total design area for each charge pump is 1 nF and the size of the load capacitor C_{load} is 10 nF.

Another important issue in charge pump operation is the switching frequency. While charge boosting is performed at frequencies within 10–30 MHz depending on the desired load current, the frequency should be reduced to less than 100 kHz when operating in a standby mode in order to save the energy. A complete study of the switching frequency in relation to the load requirements was presented in [7]. Frequency regulation should be also related to transistor sizing for efficient transfer of energy from the source to the load. These issues must be considered at the practical implementation of the voltage doubler charge pumps in CMOS technology.

V. VLSI Design of a Voltage Doubler

Practical design of a charge pump addresses a number of issues related to the specific implementation technology. In order to validate results of our analysis and design considerations a two-stage MPVD was implemented in the Orbit 2.0-μm CMOS technology using MOSIS Fabrication Service[1] . The die size is 2220×2250 μm^2. To improve the power transfer efficiency, especially in the light load condition, a frequency regulator was used to regulate switching frequency. The schematic design, layout and simulation results presented were obtained using Mentor Graphics tools.

General organization of the two-stage MPVD is shown in Fig. 20. The designed charge pump consists of two main parts. The first one generates the clock pairs used to control the switches of the charge pump. The clock pairs generator includes the frequency regulation circuit. The second part is the two-stage charging circuit, which delivers charge to the output load at the increased voltage $V+$.

In a practical implementation, a number of issues related to parasitic capacitances, leakage resistances and clock signals have to be considered. First of all, a power loss in the charge pump must be minimized both to protect the integrated circuit from overheating and to improve pump efficiency. Most of the resistive power loss results from current through the MOS transistor switches, and dynamic power loss occurs as a result of switching charge pump capacitances. Choosing a large ratio of W/L reduces the turn-on transistor resistances and the resistive power loss. This, however, increases dynamic power losses.

There are two main components of the dynamic power losses in this switching circuit. One is the power loss in charging and discharging the MOS gates, and the other one is the loss in diffusion capacitors of the source-bulk and the drain-bulk pn-junctions. Since the controlling clock pairs have different frequencies, (all of them with amplitude $V+$), the switching power loss in gate capacitors P_G is given by

$$P_G = \frac{C_{ox}V+^2}{T}\sum_{i=1}^{4} W_i L_i + \frac{C_{ox}V+^2}{2T}\sum_{j=5}^{8} W_j L_j. \qquad (16)$$

Every MOS transistor in the charging circuit has voltage level varying pn-junctions which cause the dynamic power loss P_{DS} proportional to the drain/source capacitance of MOS transistors. The dynamic power loss is the sum of P_G and P_{DS} and depends on the frequency and the values of W and L of the switching transistors. The W/L ratio have to be optimized to minimize total power losses in the switching circuit. The optimized W in our design equals to 3000 μm for NMOS and 6000 μm for PMOS with L set to 2 μm—the minimum allowed for this technology.

When the load becomes lighter, the current through transistors decreases, which reduces the resistive power loss. The factors affecting the dynamic power loss do not change. As a result, the ratio of the output power to power loss decreases, which reduces the pumping efficiency. Even in the no load condition, the charge pump still dissipates a dynamic power, and the power efficiency is 0%. To address this problem, the switching frequency must be lowered by using the frequency regulator shown in Fig. 21.

The frequency regulator circuit has 12 transistors. The left part (transistors M1 to M4) is the core of the circuit, and is used to convert the frequency and shift the voltage level of the clock to $V+$. The middle part (transistors M5 to M8) is designed to obtain a sharp clock waveform. The right part (transistors M9 to M12) is used to shift the clock voltage level to VIN.

This circuit has two stable states. We define time to change from one state to another as the response time. If half of the clock period T of CK is longer than the response time, the circuit oscillates between these two states. Otherwise, the circuit stays in a stable state. The ratios of the 12 transistors are selected to make the response time close to 25 us when $V+$ is 12.5 V (with VIN equal to 3.3 V). Simulation results (Fig. 22) reveal that a

[1]The MOSIS Service Information Sciences Institute, University of Southern California, 4676 Admiralty Way, Marina del Rey, CA 90292–6695.

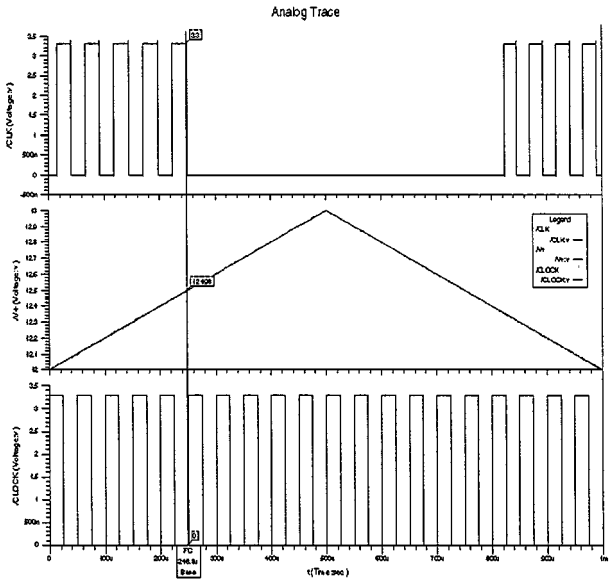

Fig. 22. Simulation result of the frequency regulator.

TABLE II
SIMULATION RESULTS OF $V+$ AND POWER EFFICIENCY WITH DIFFERENT LOAD RESISTORS

MPVD without frequency regulation				
RL(Ohm)	V+ (V)	Pin(mW)	Pout(mW)	Efficiency(%)
no load	13.18	1.85	0	0
100K	13.16	3.85	1.73	44.9
50K	13.11	5.32	3.44	64.7
20K	12.92	10.5	8.36	79.6
10K	12.55	18.9	15.8	83.6
5K	11.87	33.7	28.5	84.6
2K	9.75	73.2	47.9	65.4
1K	7.46	134	56.2	41.9
500	5.11	255	53.3	20.9
MPVD with frequency regulation				
RL(Ohm)	V+ (V)	Pin(mW)	Pout(mW)	Efficiency (%)
no load	12.5	0.083	0	0
100K	12.5	1.75	1.56	89.1
50K	12.5	3.43	3.13	91.3
20K	12.5	8.46	7.81	92.3
10K	12.5	17.2	15.6	90.7
5K	11.87	33.7	28.3	84.0
2K	9.75	73.5	47.6	64.8
1K	7.46	134	56.1	41.9
500	5.11	255	53.3	20.9

higher $V+$ results in a longer response time. When $V+$ drops below 12.39 V, as a result of the charge used to drive the load and to cover the power loss in the circuit, CLK oscillates again.

Table II shows the test results of the two-stage MPVD with different load resistors.

P_{in} represents power supplied by VIN and P_{out} is the output power. The upper part shows the results without the frequency regulation, in which the $V+$ decreases with the decreasing load resistance, dropping to 5.11 V for 500Ω. When the load is about 1 kΩ, the output power is at its maximum value of 56.2 mW, but the power efficiency is only 41.9%. This large power loss can harm the integrated circuit during switching. The maximum power efficiency (84.6%) occurs when the load resistor is 5 kΩ.

The lower part of Table II shows the results with the frequency regulation. When the load resistor is no more than 5 kΩ, the results are almost identical as those without the frequency regulation. When the load becomes lighter, the output voltage stays at 12.50 V, resulting in the output power being a little lower than it was without the frequency regulation. Nevertheless, the power efficiency is dramatically improved. When there is no load, even the power efficiency is 0%, but the input power is only 0.083mW, while without the frequency regulator it is 1.85 mW. This means that the power loss was reduced by a factor of 22. We can also see from Table II, that a steady voltage output of 12.5 V is obtained when the load resistance is larger than 10 kΩ. A stable level of the output voltage with different load values is another advantage of using the frequency regulation.

Test of the fabricated designs confirmed the simulation-based results. Due to the low breakdown voltage the chips were tested using VIN equal to 2.3 V. The output voltage reached 8.93 V, which corresponds to 3.88 voltage gain. The maximum power delivered to 1 kΩ load was 19.34 mW with the maximum power transfer efficiency equal to 85.5%.

VI. CONCLUSION

Novel organizations of the switched-capacitor charge pump based on voltage doublers and charge pump design issues are discussed in this paper. The TPVD charge pumps work with two inverted clocks similar to Dickson and Makowski charge pumps. The MPVD charge pumps reach a specified voltage gain with the least number of capacitors, but require more sophisticated clocking scheme. An extensive computer simulation of voltage doublers was performed to observe effects of the resistive load, capacitance ratio, and clock frequency on the levels of the output voltage and power. Load conditions for the optimum power transfer were established. Charge pump simulation was performed using a Q–V based simulator SAMOC. Comparing with two other switched-capacitor charge pumps, Dickson and Makowski, the voltage doublers use yet fewer stages but have longer rise time and deliver relatively less power. An experimental two-stage MPVD charge pump with the frequency regulation circuit was designed, fabricated, and tested.

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