An Adaptive Routing Algorithm to Improve Lifetime Reliability in NoCs Architecture

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***Abstract*—According to Moore's Law, the number of transistors on a single chip doubles every two years, allowing tens or even hundreds of cores to be integrated. As multi-cores communicate with memory, the underlying Network-on-Chip (NoC) experiences different stress levels due to asymmetric traffic patterns and complex routing algorithms. Unfortunately, the growth in the number of transistors in NoCs will significantly impact both reliability (physical failures) and aging (uneven utilization) due to the increasing effects of Electromigration (EM), Hot carrier injection (HCI) and Negative Bias Temperature Instability (NBTI). In this paper, we propose a novel in-flight, adaptive, routing algorithm to reduce the accumulation of EM, HCI, and NBTI effects on the lifetime of NoC. The proposed routing algorithm is based on a new metric called Packet-Per-Port (P^3) which equalizes the stress throughout the network. The net impact is that the network components such as the links and the routers will age evenly and thereby improve NoC reliability and maximize the lifetime of the chip. Our results indicated that for Splash-2 traces, we observe 7.3% to 13.7% energy per bit reduction and up to 6.23% improvement in the transistor reliability when compared to Dimensional Order Routing (DOR) on 8x8 mesh.**

I. Introduction

Network-on-Chips (NoCs) has emerged as a potential solution that can deliver the required performance for multi-core applications in terms of latency, throughput, and low power consumption. To improve the reliability of transistors, it is important to incorporate techniques to decelerate the aging effects in order to increase the Mean-Time-To-Fail (MTTF) and improve system reliability. Aging is a major cause for system failure; threshold voltage V_{th} increases due to aging, which in turn increases the gate delay. When cumulative gate delay of a router's critical path increases by 10%, the system fails to operate under the specified timing constraints [1]. Aging can be attributed to the percentage of transistor utilization. Aging is due to three factors that primarily affect the transistor: (1) NBTI - PMOS transistor seeing logical zero that stresses the transistor; (2) HCI - occurs due to flow of injected carries to the gate that achieve higher kinetic energy and thereby shift the Vth gradually, and (3) EM - electrons diffuse with ions and lose some energy which creates voids and traps charges, thereby reducing the efficiency of the connection.

Prior work on aging in NoCs has developed a wear-resistant router micro-architecture that reduces the aging effects by adding an exercise circuit to generate random cycle when the router is idle [2], under the assumption that real traffic demonstrates low utilization. Bardwaj et al. [3] investigated aging in NoCs and proposed an age aware routing algorithm to decrease the aging process and improve the lifetime of NoCs. The algorithm considers aging and congestion on route selection, since the aging effects can be recovered they implement recovery cycle after pre determined value. To reduce the power consumption, Bhardwaj et al. [4] proposed mixed integer liner programming based on oblivious routing algorithm which considers the power consumption while selecting the routing path. While prior works have proposed various mechanisms to reduce aging, adaptive routing algorithm with minimal path selection had not been proposed.

In this paper, we propose an in-flight adaptive routing algorithm which works on aging links and routers of the network at the same pace to reduce the aging effects and increase the lifetime of the chip. The algorithm works by distributing the load throughout the network with minimal effects on the network performance. We propose Packet Per Port (P^3) as an aging metric which is paired with an adaptive routing algorithm to deliver better distribution of the network load. The algorithm takes advantage of the fully adaptive routing to avoid the aged link and routers in-flight. P^3 connects the router age and the link age to the time they are being used making it possible to control both ages at once to improve the lifetime of chip. The use of this simple but effective aging metric allows us to improve the transistor reliability by 3.6% to 6.27% when compared to DOR. We obtain up to 13.8% reduction in power consumption.

II. Aging Reduction Mechanism: Packets Per Port (P^3)

In this section, we describe the proposed P^3 based routing algorithm and the power-efficient router micro-architecture

A. Age-Aware Routing

Oblivious routing algorithms that ignore the network load when choosing the output port of the router are simple, but create hot spots due to routers experiencing unequal utilization. Routers that are lowly utilized suffer from high NBTI effects whereas highly utilized links suffer from EM effects. On the other hand, fully adaptive routing algorithms can distribute the load better on routers and links and equalize the utilization, however the penalty shows up in routing complexity and excess power and latency consumption due to additional hops. For the above reasons, we propose a new routing algorithm that is fully adaptive and yet uses minimal number of hops to transfer a packet. The proposed routing algorithm takes advantages of both worlds (oblivious and adaptive) to improve

the lifetime of chips by reducing the NBTI/EM effects on routers/links while delivering high performance.

The routing algorithm makes routing decisions based on two primarily scores: P^3 and congestion score. P^3 is a directional metric that provides the utilization information of the next routers locally. The number of free buffer slots propagates dimensionally, either row-wise or column-wise to form the congestion score. To minimize the lag time between the transmission of the congestion information and the decision making, we confined the congestion information to the boundaries of source and destination nodes within a grid. Every node receives congestion scores from each node along the dimension rather than one cumulative score as in 1D-RCA [11]. The node then crunches the number to decide the congestion score. The sending router requests and receives congestion information from the two possible routing directions (x and y) to reach the destination router. However, in 1D RCA the congestion information is not bounded by the area of interest, as the router receives congestion information along the entire row or column of the NoC which increases the lag time between receiving the congestion information and making the decision. Moreover, traffic intensities could change due to variations in application behavior making 1D-RCA slower to respond to transient traffic changes. Therefore, our proposed routing algorithm improves on reducing the lag time to receive congestion score and improves the congestion score calculation as it is limited to source and destination nodes and not the entire network.

Independent, smaller crossbars have been implemented to optimize the power consumption, and reduce the area as the wires are shorter and can deliver better throughput [5]. The router's age is determined by the delay variation in the critical path, and therefore, the use of smaller crossbars will not impact aging. However, the use of multi-crossbars within the router micro-architecture increases the probability of an output port being occupied when compared to the conventional router [5]. The proposed micro-architecture with split crossbars along with congestion and aging score calculation is shown in Figure 1.

Virtual Channel (VC) allocation is critical in NoCs as it prohibits any circular dependencies therefore prevents any deadlock/livelock. In routers with multi-crossbars presents the four quadrants (+x,+y), (+x,-y), (-x,+y), and (-x,-y), where the packets can be adaptively routed to the destination quadrant, assuming that the source is the reference point. As Figure 1 shows, we require four VCs to eliminate deadlocks/livelocks with each VC allocated to one quadrant. The VC allocation is based on the destination quadrant, if the destination is in the (+x,+y) quadrant, VC1 gets allocated. If the destination is in the (+x,-y), VC2 gets allocated and so on. This separation creates four Virtual Networks (VN) accordingly, and packets get injected to one VN and cannot exit until the packet reaches its destination. Forcing packets to stay within the assigned VN allows packets to move freely within the assigned VN and be routed adaptively.

B. Routing Algorithm

The routing algorithm selects the least utilized as well as the least congested link with higher priority given to least utilized link. The route computation includes two stages: any source/destination combinations that are not located in the same row/column have two possible links/routers. We used the number of free input buffers slots to calculate the propagation congestion. We decided to utilize a 1-dimensional RCA as $X_{Cong} = \sum_{N=xsrc}^{xdest} \frac{Xrouter_{FBS}}{|xoffset|}$ and $Y_{Cong} = \sum_{N=ysrc}^{ydest} \frac{Yrouter_{FBS}}{|yoffset|}$.[1] We used utilization as an aging metric. At each router, the links/routers utilization are determined as XP^3 = P^3[Router][$X_{direction}$] along the x-axis and $YP^3 = P^3[Router][Y_{direction}]$ along the y-axis. Both aging scores and the dimensional congestion scores are being fed to the routing algorithm. Next section illustrates all the decisions in the routing algorithm.

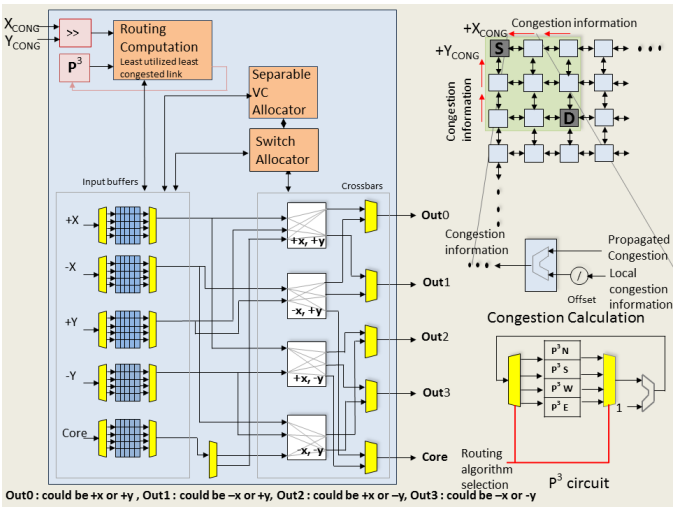


Fig. 1: Proposed Router Microarchitecture.

	Inputs: Coordinate of current router (Xsrc,Ysrc) and of destination router (Xdest,Ydest) X_{Cong}, Y_{Cong}, XP^3, YP^3
1.	Calculate Xoffset = Xdest - Xsrc
2.	Calculate Yoffset = Ydest - Ysrc
3.	no. of hops = abs(Xoffest) + abs(Yoffset)
4.	Determine the Virtual Network [X/Y , -X/Y , X/-Y , -X/-Y] the packet is going to be routed in
5.	**If**($XP^3 > YP^3$) Output port = $Y_{direction}$ **Else If**($XP^3 < YP^3$) Output port = $X_{direction}$ **Else If**($XP^3 == YP^3$) **If**($X_{Cong} <= Y_{Cong}$) = Output port = $X_{direction}$ **Else** Output port = $Y_{direction}$
6.	(Output port == $X_{direction}$) ? Xoffset−− : Yoffset−−
7.	(Output port == $X_{direction}$) ? P^3[Router][$X_{direction}$]++ : P^3[Router][$Y_{direction}$]++
8.	While (no. of hops != 0)

TABLE I: P^3 Routing Algorithm

C. Routing Example

In this section, we illustrate with an example our proposed P^3 routing algorithm. As shown in Figure 2, the example depicts a 4x4 mesh architecture, however it can be applicable to 8 x 8 architecture as well. In our example router 15 (the

[1] where Xrouter is the next router on the X-axis, Yrouter is the next router on Y-axis and FBS is Free Buffer Slots.

top right corner) wants to communicate with router 0 (bottom left corner). At the source node as shown in Figure 2(a), R15 (located at [3,3]), wants to communicate with the destination router R0 (located at [0,0]) and the x and y offsets are [-3,-3]. We use red color for highly congested links and higher P^3 values, blue color for lower P^3 values, black colored routers for routers through which packets have traversed, black solid lines for links that the packet has, and black dashed lines for next possible links. Based on the colors code (from the Figure 2) we can see that R14 on Y-axis is utilized higher than the R11 on the X-axis. R15 receives congestion information from both -X, and -Y axes, R15 senses congestion (between R12 and R13 on the X-axis, and between R7 and R11 on the Y-axis). Since congestion calculation is based on the distance between the congestion and the source, X_{Cong} will be lower than the Y_{Cong}. The routing algorithm routes the packet to the least utilized and the least congested link and $P^3[R15][-X]$ will be increased by 1. As shown in Figure 2(b) for R14, the next router on the X-axis is R13, and on the Y-axis is R10. In terms of utilization, R13 is preferred and in terms of congestion R10 is preferred. As we prioritize utilization over congestion, R13 is selected by the routing algorithm and $P^3[R14][-X]$ is increased by 1. As shown in Figure 2(c), R12 and R9 are the next possible candidate routers for the packet. The algorithm selects to make a turn to the Y-direction since R12 has higher utilization when compared to R9 and increase $P^3[R13][-Y]$ by 1. Even though it senses congestion along the Y-axis, priority is given to utilization rather than congestion. As shown in Figure 2(d), the two possible routers (R8 and R5) are potential candidates for the packet, the algorithm decides to take the least utilized router as it is R5 and increase $P^3[R9][-Y]$ by 1. The routing decision continues in similar fashion until packet reaches its destination.

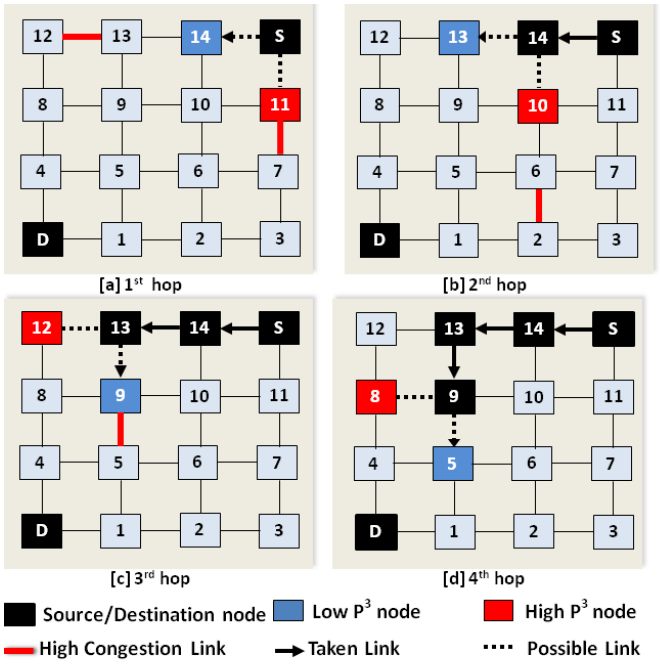


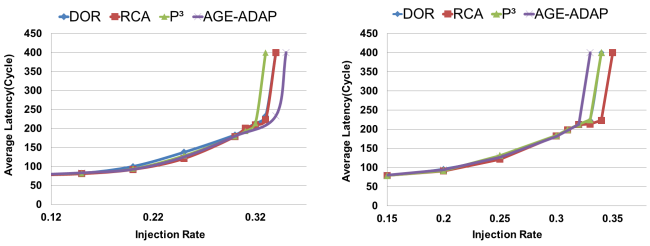
Fig. 2: P^3 Routing Example, each figure demonstrates a one hop transfer.

III. Experimental Methodology and Results

We use a cycle accurate network simulator that models the router microarchitecture presented in section II. We compared our routing algorithm to three routing algorithms: (1) Dimensional Order Routing (DOR), (2) Regional Congestion Awareness (RCA), and (3) Age-Aware Adaptive Routing (AGE-ADAP) proposed in [3] where packets are being routed to the least aged and least congested path using look-up table. While we compared all three algorithms to P^3 on a 4 x 4 mesh, we did not compare AGE-ADAP for 8 x 8 mesh. This is due to the fact that AGE-ADAP was designed on a 4x4 mesh with a concentration of 4 and our design is applicable to designs without any concentration. For the simulation, we used four VCs allocated separately. Synthetic and real traffic (Splash-2) are used for evaluating the performance of all routing algorithms.

To model the aging effects we modeled a 45 nm transistor on Synopsys HSPICE using HCI/NBTI long term degradation and Predictive Technology Models (PTM) [6] for 10 years. We observed the change in threshold voltage to model the aging factor as presented by [7].

Latency: Figure 3 shows the network latency for 4 x 4 mesh architecture for matrix transpose and bit reversal traffic pattern. DOR provides the best performance for complement and uniform traffic since the load is well distributed throughout the network. This is due to the fact that adaptive routing algorithms will try to balance the load on the peripheral routers which results in traffic diverted to the core routers where congestion builds up. However, since RCA is only concerned with congestion, it outperforms P^3 when the network load is uneven as shown in 3. It must be noted that RCA does not distribute the load evenly throughout the network and the packet simply chooses the least congested path. Even though P^3 does not deliver the lowest latency, P^3 improves the distribution of load which will increase the lifetime of the chip. As P^3 is concerned with load distribution and congestion avoidance, latency impact is minimal. AGE-ADAP is able to outperform P^3 in terms of latency, as it is not a fully adaptive algorithm, however AGE-ADAP does not distribute the load as P^3.



(a) Matrix Transpose (b) Bit Reversal

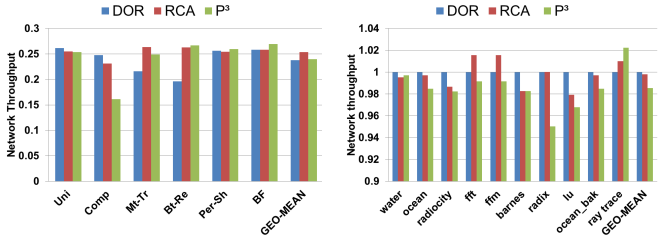
Fig. 3: Average network latency for 4 x 4 mesh for a few select synthetic traffic patterns - (a) Matrix Transpose , (b) Bit Reversal.

For 8 x 8 mesh, P^3 shows better load distribution as well as improves the network latency. P^3 outperforms DOR for permutation traffic, 19% for matrix transpose and 77% bit reversal because it is able to avoid congestion and load balance

the traffic throughout the network. However, RCA showed better network latency as it does not consider utilization, and only avoids congestion.

Throughput: For 4 x 4 mesh the results indicates that P^3 did not affect the throughput for all tested traffic patterns except for complement traffic where P^3 reduces the throughput by 10%. However for 8 x 8 mesh as shown in Figure 4(a), P^3 is able to improve the throughput by 36% when compared to DOR for bit reversal traffic. As complement traffic is well distributed throughout the network, throughput is affected because of the increased congestion at the core routers. Real traffic throughput as shown in Figure 4(b) indicates that the throughput degradation is marginal and depends on traffic distribution.

Aging:



(a) 8x8 mesh (synthetic traffic) (b) 8x8 mesh (Splash-2 traces)

Fig. 4: Network throughput - (a) 8x8 mesh under synthetic traffic patterns, and (b) 8x8 mesh under Splach-2 traces (normalize to DOR). (notation: Uni: Uniform, Comp: Complement, Mt-Tr: Matrix Transpose, Bt-Re: Bit Reversal, Per-sh: Perfect Shuffle, BF: Butterfly, GEO-MEAN: Geometric Mean).

Aging in NoCs can be determined by the slow shift in the threshold voltage V_{th} and this will result in an increase in gate delay. As NoCs is a latency sensitive network, increasing the critical path delay by more than 10% is considered as a system failure [1]. The latency induced will exceed the router pipeline which will create erroneous packet reception. Based on reaction-diffusion, transistor delay is shifted by V_{th} according to Alpha Power Law[8] : $d_g \alpha \frac{V_{dd}}{\mu(V_{dd}-V_{th})^{\varphi}}$

P^3 will control the increase of the threshold voltage by dividing the load throughout the network to reduce the age degradation. P^3 was able to achieve a better utilization and a shorter duty cycle. We ran Synopsys HSPICE for a transistor model under PTM for 10 years and collected the V_{th} to calculate aging[7] as described $Aging = \frac{\triangle V_{th}}{V_{th}}$.By increasing the load on the peripheral routers and decreasing the load on the core routers, P^3 showed the best load distribution through out the network. As shown in Figure [5], P^3 is able to increase the lifetime reliability by decreasing the diffusion of the threshold voltage.

Energy Per Bit: The use of multi-crossbars within the routers and the distributed routing algorithm paid off for P^3 in terms of energy per bit. Figure 6 shows that P^3 consumes the least energy per bit for Splash-2 traces, P^3 reduces the energy per bit between 7.3% and 13.7%. All simulation has been done on DSENT simulator [9].

IV. CONCLUSIONS

In this paper, we propose an in-flight adaptive routing algorithm that improves the lifetime of the network by leveling the load on the network. By distributing the load on all links and routers, our evaluation showed that we can reduce the delay variation and improve the reliability of the chip. Our results also indicate that we can reduce the power consumption when compared to state-of-the-art routing algorithms with marginal performance degradation.

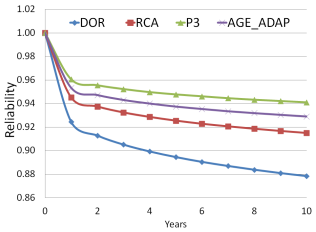


Fig. 5: The aging effects on transistor reliability.

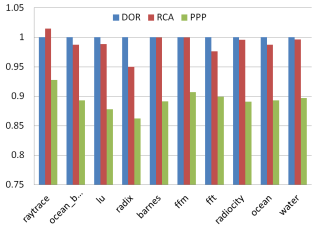


Fig. 6: Energy per Bit for Splash-2 traces normalized to DOR.

V. ACKNOWLEDGMENT

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REFERENCES

[1] J. McPherson, *Reliability Physics and Engineering: Time-To-Failure Modeling*. Spring, 2010.

[2] H. Kim, A. Vitkovskiy, P. V. Gratz, and V. Soteriou, "Use it or lose it: Wear-out and lifetime in future chip multiprocessors," in *Proceedings of the 46th Annual IEEE/ACM International Symposium on Microarchitecture*. ACM, 2013, pp. 136–147.

[3] K. Bhardwaj, K. Chakraborty, and S. Roy, "Towards graceful aging degradation in nocs through an adaptive routing algorithm," in *Design Automation Conference (DAC), 2012 49th ACM/EDAC/IEEE*, June 2012, pp. 382–391.

[4] Bhardwaj, K. and Chakraborty, K. and Roy, S., "An milp-based aging-aware routing algorithm for nocs," in *Design, Automation Test in Europe Conference Exhibition (DATE)*, March 2012, pp. 326–331.

[5] A. Kodi, R. Morris, D. DiTomaso, A. Sarathy, and A. Louri, "Co-design of channel buffers and crossbar organizations in nocs architectures," in *Computer-Aided Design (ICCAD), 2011 IEEE/ACM International Conference on*, Nov 2011, pp. 219–226.

[6] "Predictive technology model," http://ptm.asu.edu/.

[7] Y. Wang, S. Cotofana, and L. Fang, "A unified aging model of nbti and hci degradation towards lifetime reliability management for nanoscale mosfet circuits," in *Nanoscale Architectures (NANOARCH), 2011 IEEE/ACM International Symposium on*, June 2011, pp. 175–180.

[8] T. Sakurai and A. R. Newton, "Alpha-power law mosfet model and its applications to cmos inverter delay and other formulas," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr 1990.

[9] C. Sun, C. H. O. Chen, G. Kurian, L. Wei, J. Miller, A. Agarwal, L. S. Peh, and V. Stojanovic, "Dsent - a tool connecting emerging photonics with electronics for opto-electronic networks-on-chip modeling," in *Networks on Chip (NoCS), 2012 Sixth IEEE/ACM International Symposium on*, May 2012, pp. 201–210.

[10] Bhardwaj, S. and Wenping Wang and Vattikonda, R. and Yu Cao and Vrudhula, S., "Predictive modeling of the nbti effect for reliable design," in *Custom Integrated Circuits Conference, 2006. CICC '06. IEEE*, Sept 2006, pp. 189–192.

[11] P. Gratz, B. Grot, and S. W. Keckler, "Regional congestion awareness for load balance in networks-on-chip," in *High Performance Computer Architecture, 2008. HPCA 2008. IEEE 14th International Symposium on*, Feb 2008, pp. 203–214.