

EE 4683/5683: Computer Architecture
Project # 2

Instructions:

- 1) Use Dinero simulator to solve problems 1-4.
- 2) Submit a PDF of your analysis of the data and your results. One sample output per question can be attached at the end of the solution as appendix. Do not put all the runs of all the simulation outputs.

Question 1: Calculate the Local and Global Miss Rates (Use cc1.din and spice.din)

Calculate the global and local miss rates for a 2-level cache. Consider level-1 cache with 16KB and vary the level-2 cache size from 2KB, 8KB, 32KB and 128KB for a block size of 16bytes, LRU replacement policy and 2-way associativity. Compare this value with the miss rates of single-level cache.

- a) Consider only data caches for simulation and plot the results (Logarithmic scale makes the plot clearer).
- b) What conclusion can you draw from this?
- c) Is the local miss rate a good measure of secondary caches?
- d) What is the optimum value of the secondary cache size?

Question 2: Unified and split caches

(use cc1.din only)

Compare the cache miss ratios of the following two systems:

- a system with a 32K-byte unified cache
- a system with a 16K-byte instruction-only cache and a 16K-byte data-only cache.

Assume the caches are 4-way set associative, LRU replacement policy and the block size is 32 bytes. What conclusions can you draw from this experiment?

Question 3: Multi-level L2 Cache

(use spice.din only)

Calculate the AMAT for 2-level cache with:

- (a) level-1 cache size of 16KB and level-2 cache size of 64KB
- (b) level-1 cache size of 32KB and level-2 cache size of 128KB

Assume direct-mapped for level-1 and 4-way set-associative for level-2 with block size of 16 bytes. The hit time for level-1 is 1 clock cycle and for level-2 is 8 clock cycles. Let the miss

penalty for level-2 be 50 clock cycles and memory access latency be 100 clock cycles. What can you say about the performance of the two organizations?

Question 4: Calculation of CPI (use all 3 traces)

Calculate the Effective CPI of a 2-level cache hierarchy with level-1 direct-mapped cache of 4KB and level-2, 2-way set associative cache of 64KB with the block size of 32 bytes for both caches. The base CPI is assumed to be 1.5 and there are 1.45 memory references per instruction. The hit time to level-1 is 1 clock cycle and hit-time to level-2 is 15 clock cycles. The miss penalty for level-2 is assumed to be 60 clock cycles.

[Hint:

Average Memory stalls/instruction =

Misses/instruction (L1) \times Hit Time (L2) + Misses/Instruction (L2) \times Miss Penalty (L2)

Misses/Instruction (L1) = Miss Rate (L1) \times Memory Access/Instruction

Misses/Instruction (L2) = Miss Rate (L2) \times Memory Access/Instruction]