EE 4683/5683: Computer Architecture

Homework #3

Instructions:

Graduate Students: Answer all questions.

Undergraduate Students: The last question is bonus question.

Problem 1:

3.1, 3.2, 3.3, 3.5 and 3.6 (*a, b and c*)

Problem 2

3.14 (*a, b and c*)

Problem 3:

The main memory of a computer is organized as 256 blocks, with a block size of 8 words. The cache has 16 block frames. For the questions below, show the mappings from the numbered blocks of main memory to block frames of the cache. Draw all lines showing the mappings as clearly as possible.

a) Show the direct mapping and the address bits that identify the tag field, the index field, and the word offset field (the bits identifying a word within a block).

b) Show the fully associative mapping and the address bits that identify the tag field and the word offset field.

c) Show the mapping for the 2-way set associative mapping and the address bits that identify the tag field, the set number, and the word number.

Problem 4

Consider a memory system with a two-level hierarchy with a cache M1 and main memory M2. The size of the main memory, M2 is 256 bytes with block size of 16 bytes. The size of the cache, M1 is 64 bytes with the same block size of 16 bytes. The word length is 4 bytes, implying 4 words per block. A certain trace program generates the following sequence of word addresses,

0,8,16,1,24,21,20,3,32,61,31,19,16,60,28,21,8,11,19,22,28,42,55,58,59

Note, every time a new block is accessed by the cache, up to 4 words are received implying that if block 0 is accessed from the main memory then 0,1,2,3 words are obtained, if block 1 is accessed from the main memory, words 4,5,6,7 are obtained, if block 2 is accessed from the main memory words 8,9,10,11 are obtained and so on. The addresses given above are word addresses, not memory block addresses. Assume that the access time is 2 clocks from the cache (M1) and 50 clocks from main memory (M2), the transfer rate is 4 bytes per clock and that 25% of the transfers are dirty. The base CPI of a perfect memory system is 1.75.

(a) Consider a fully associative cache with LRU replacement policy. Determine the hit ratio. What is the average memory access time?

(b) Consider a direct mapped cache. Determine the hit ratio. What is the average memory access time?

Problem 5 *For Graduate students, Undergrads get BONUS if solution is correct!*

You purchased an Acme computer with the following features

- 95% of all memory accesses are found in the cache
- each cache block is two words, and the whole block is read on any miss
- the processor sends references to its cache at the rate of 10^9 words per second
- 25% of those references are writes
- assume that the memory system can support 10^9 words per second, reads or writes
- the bus reads or writes a single word at a time (the memory system cannot read or wrote two words at once)
- assume at any one time, 30% of the blocks in the cache have been modified
- the cache uses write allocate on a write miss

You are considering adding a peripheral to the system, and you want to know how much of the memory system bandwidth is already used. Calculate the percentage of memory system bandwidth used on the average in the two cases below. Be sure to state your assumptions

a. The cache is write through

b. The cache is write back