EE467/567 "Advanced Microprocessors"

Assignment # 4
Due: in-class Friday March 9, 2012

Problem 1:

(a) If DS = 0103_{16} in a protected mode system, what is the requested privilege level and which entry in the descriptor table is selected?

(b) Given a program stored in a code segment with (CS) = 128BH. If the program tries to access a data segment with (DS) = 1A00H. The affiliated Descriptor Privilege Level of the data segment equals 2. Does a general protection fault (#GP) occur? Explain your answer!

(c) In each of the following cases explain if a General Protection Fault occurs:

- A non-conforming code segment with a CPL=3 tries to access a piece of code located in a code segment with a DPL=2 and RPL=3?
- A conforming code segment with a CPL=2 tries to access a piece of code located in a code segment with a DPL=3?

Problem 2: Given the following cache configuration for an Intel Core 2 processor:

1) 8-way set associative cache,
2) Each cache line consists of 16 bytes,
3) Cache (L2) is 512 Kbytes in size,
4) Main memory is 256 Mbytes in size.

For each of the following consecutive instructions identify in which set of the cache the data is located after the instruction is completed. Identify if a cache hit or a cache miss occurred. Assume that initially the cache is empty. Note: the data segment DS starts at physical memory location 0x0A0000 and **real-mode** is assumed. Show your work!

Instruction	Physical Address	Set (binary)	Hit or Miss?
MOV AX, [1A34H]			
MOV BX, [1A36H]			
ADD AX, [1A40H]			
SUB BX, [20C0H]			
MOV [1A42H], AX			
MOV [20D0H], DX			

Problem 3:

Given a two-way set associative cache with 8 cache lines, and a main memory with 16 4-byte blocks (RAM = 64 bytes); 00H-03H = Block 0, etc. The computer has a 6-bit address bus and uses split cache architecture. The given cache is for data only.

Cache:

	Tag (2 bits)		Replacement policy
Set 0 (**S0**)	01	C1 C2 AC 21	12
	11	01 1C A0 11	3
Set 1 (**S1**)	00	00 00 00 12	34
	01	00 10 00 12	22
Set 2 (**S2**)	10	11 2E FF 22	8
			-
Set 3 (**S3**)			-
			-

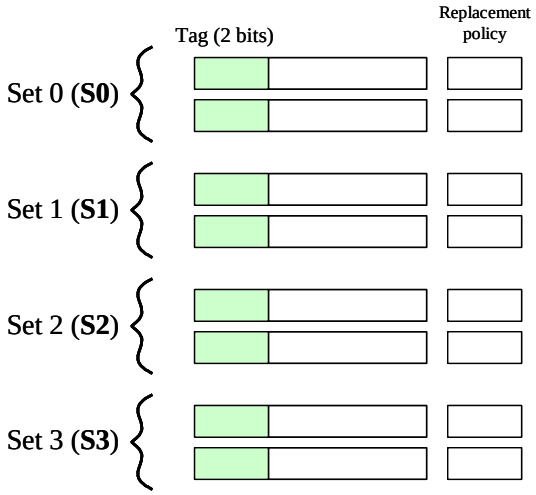
Main Memory:

	Memory Locations:
01 22 A0 11	00H – 03H
00 00 00 12	04H – 07H
01 AA A2 11	08H – 0BH
A0 A0 B0 12	0CH – 0FH
C1 C2 AC 21	10H – 13H
00 10 00 12	14H – 17H
01 AA A0 11	18H – 1BH
11 00 B3 12	1CH – 1FH
01 24 50 11	20H – 23H
01 03 07 1A	24H – 27H
11 2E FF 22	28H – 2BH
02 00 00 00	2CH – 2FH
01 1C A0 11	30H – 33H
AF EF 0D 12	34H – 37H
2E 2B AC 11	38H – 3BH
00 05 00 12	3CH – 3FH

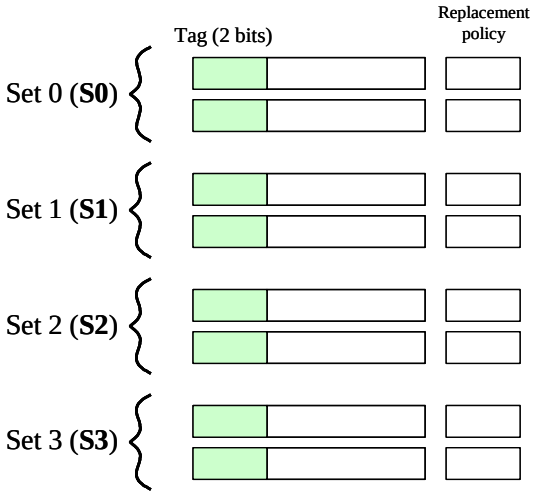
Given that the numbers in the replacement column represent the times in microseconds elapsed since the last time a byte in that cache line was accessed. Using a Least Recently Used (LRU) replacement policy, show how the cache contents change after each of the following lines of assembly code (indicate if a cache hit or cache miss occurred). The contents of DS are 00. Furthermore, assume that each instruction takes 1 microsecond.

```
Line 1: MOV   AX, [09H]
Line 2: ADD   AX, [28H]
Line 3: MOV   [25H], AX
Line 4: MOV   BX,[3EH]
Line 5: ADD   BX, 15H
Line 6: MOV   [29H],BX
```

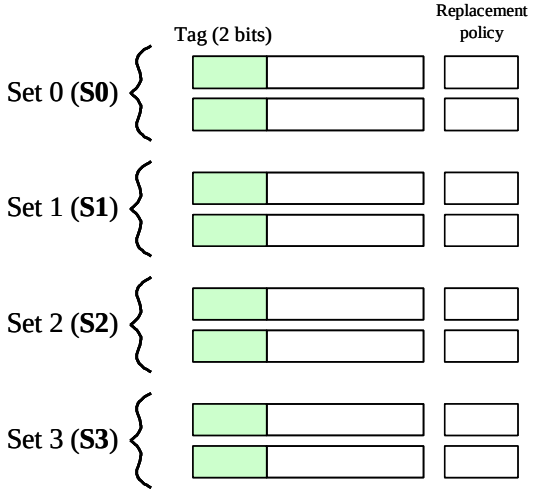
Cache after source code line 1:



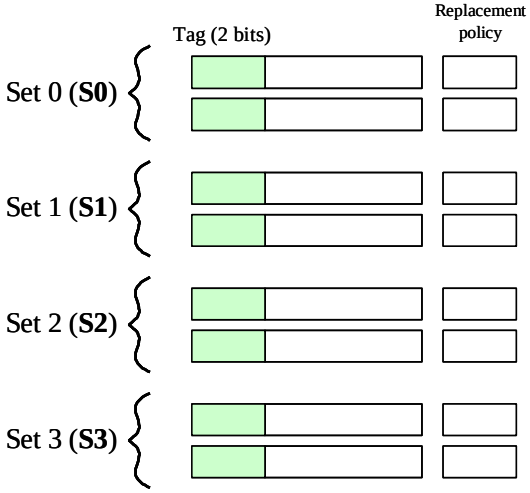
Cache after source code line 2:



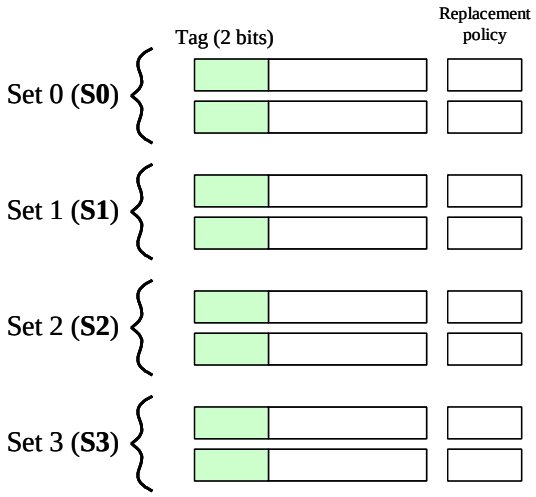
Cache after source code line 3:



Cache after source code line 4:



Cache after source code line 5:



Cache after source code line 6: