EE 3613: Computer Organization
Homework #1
Due Date: (in-class) Wednesday, September 9, 2020

Problem 1 (20 Points):

Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?
b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
c. We are trying to reduce the time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Problem 2 (15 Points):

Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D).

P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1×10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a. What is the global CPI for each implementation?
b. Find the clock cycles required in both cases.

Problem 3 (15 Points):

The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, has a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

a. For each processor find the average capacitive loads.
b. Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.
c. If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

Problem 4 (15 Points):

In the embedded market, where cost is crucial, processors sometimes implement floating point only in software. We are interested in two implementations of a computer, one with and one without special floating-point hardware.

Consider a program, P, with the following mix of operations:

Floating-point multiply: 15%
Floating-point add: 20%
Floating-point divide: 10%
Integer instructions: 55%

Computer MFP (computer with floating point) has floating-point hardware and can therefore implement the floating-point operations directly. It requires the following number of clock cycles for each instruction class:

Floating-point multiply: 6
Floating-point add: 4
Floating-point divide: 20
Integer instructions: 2

Computer MNFP (computer with no floating point) has no floating-point hardware and so must emulate the floating-point operations using integer instructions.
The integer instructions all take 2 clock cycles. The number of integer instructions needed to implement each of the floating-point operations is as follows:

Floating-point multiply: 30
Floating-point add: 20
Floating-point divide: 50

(a) Both computers have a clock rate of 1000 MHz. Find the native MIPS ratings for both computers.

(a) If the computer MFP in Exercise needs 300 million instructions for this program, how many integer instructions does the computer MNFP require for the same program?

Assuming the instruction counts from Part (b), what is the execution time (in seconds) for the program in Exercise run on MFP and MNFP?

Problem 5 (20 Points)

For this problem, suppose we have the following dynamic instruction profile for a benchmark application. The cycle count for each instruction type is listed in below.

Instruction Type	Count	Cycles
Loads	426,000,000	8
Stores	184,000,000	7
Integer ALU	662,000,000	???
Jumps	104,000,000	4
Jump and Link	52,000,000	6
Branch (taken)	328,000,000	5
Branch (not taken)	244,000,000	4

a. Compute the number of cycles for Integer ALU instructions given that the CPI is 6.006
b. Suppose a hardware improvement reduces the cycle count for ALU instructions from 6 to 4 cycles without increasing the cycle time. What is the new CPI? How much faster is the improved machine over the original machine for this benchmark?

Problem 6 (15 Points)

Assume a program requires the execution of $50X10^6$ FP instructions, $110X10^6$ INT instructions, $80X10^6$ L/S instructions, and $16X10^6$ branch instructions.
The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

a. By how much must we improve the CPI of FP instructions if we want the program to run two times faster?
b. By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?
c. By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?