EE 3613: Computer Organization

Chapter 5: The Processor: Datapath & Control - I

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Course Outline

- *CPU Performance & Evaluation*
- *Instruction Set Architecture*
- *Computer Arithmetic*
- Processor: Datapath and Control
- Pipelining
- Cache and Main Memory

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Processor: Datapath and Control

- Review: Combinational Circuits
  - Boolean algebra, basic gates, adders (done previously)
- Review: Sequential Circuits
  - Latches, Flip-Flops, Memory cell, Registers
- Verilog
  - Free versions available from Aldec and Xilinx ISE
- Datapath and Control
  - Single Cycle Datapath Implementation
  - Multiple Cycle Datapath Implementation

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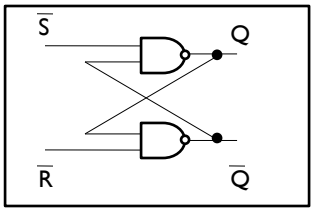
SR-Latch

Latch: The output state is changed whenever the appropriate inputs change



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1		

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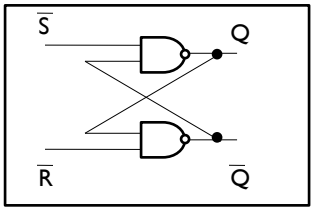
SR-Latch

Latch: The output state is changed whenever the appropriate inputs change



$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0	undefined	
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

As long as R and S remain 1, then the value of Q (and Qbar) will remain unchanged
This value is stored in this circuit – **This is the basic memory cell**

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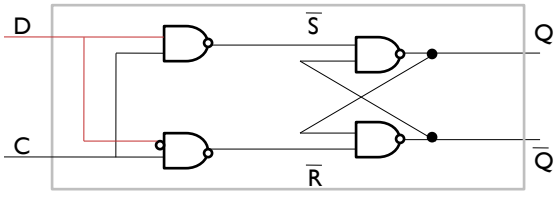
Transparent D Latch

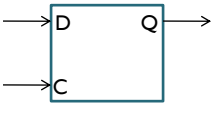
Flip-Flop: The output state is changed only on a clock edge



D	C	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	Q	$\bar{Q}$
1	1	1	0

Next state is set

State retained



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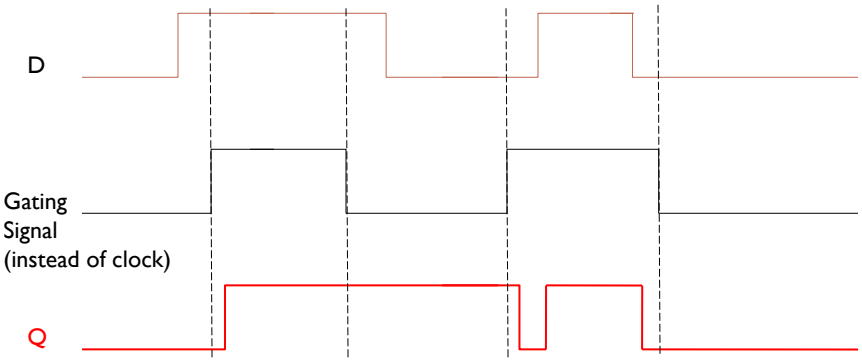
Regular D-Latch Response



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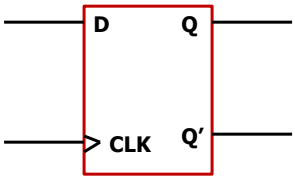
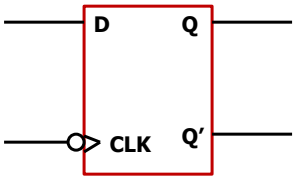
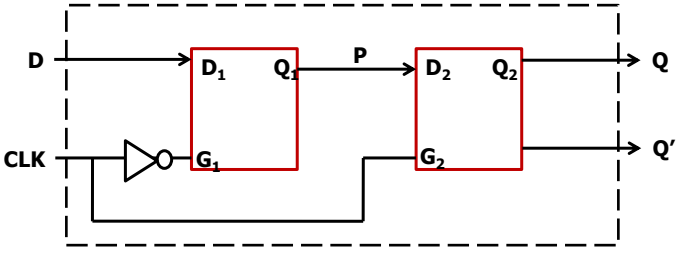
Edge-Triggered D-Flip Flop



Rising Edge Trigger



Falling Edge Trigger



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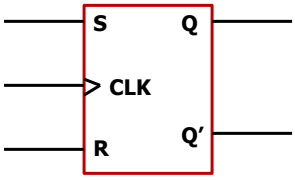
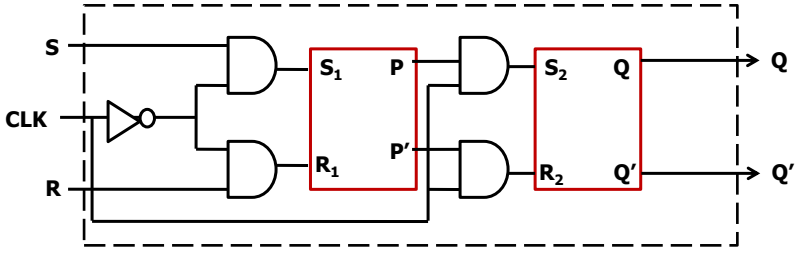
SR Flip Flop



Rising Edge Trigger

S	R	Next state (Q^+)
0	0	No Change
1	0	Q = 1, Set (after active CLK edge)
0	1	Q = 0, Reset (after active CLK edge)
1	1	Not allowed



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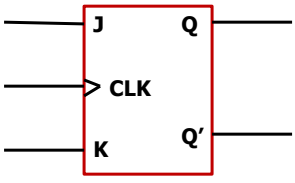
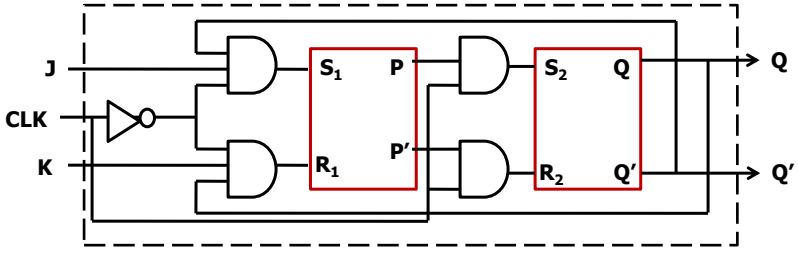
JK Flip-Flop (J = S, K = R)



Rising Edge Trigger

J	K	Next state (Q^+)
0	0	No Change
1	0	Q = 1, Set (after active CLK edge)
0	1	Q = 0, Reset (after active CLK edge)
1	1	Q′

$Q^+ = JQ' + K'Q$
(Characteristic Equation)



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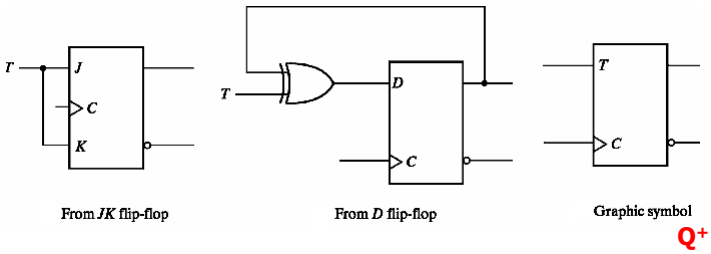
T Flip Flop

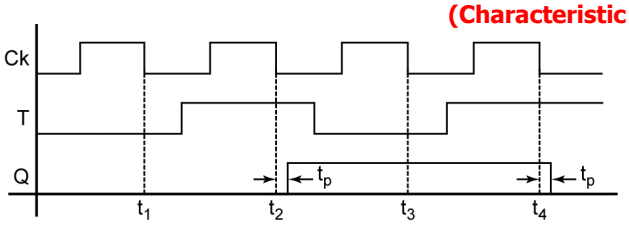
- T Flip Flop, called as Toggle FF is frequently used in building counters



TQ	Q^+
0 0	0
0 1	1
1 0	1
1 1	0

$Q^+ = T \oplus Q$
(Characteristic Equation)

Falling edge triggered



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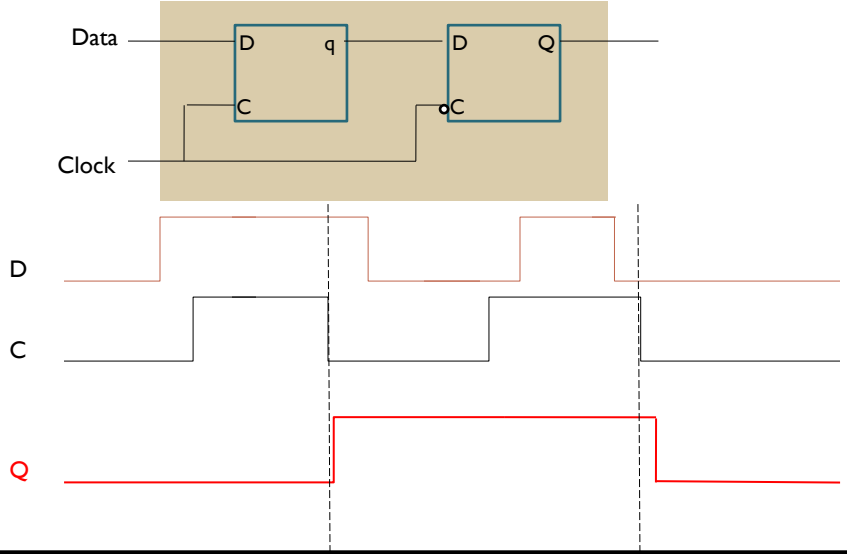
Negative Edge-Triggered (Master-Slave)



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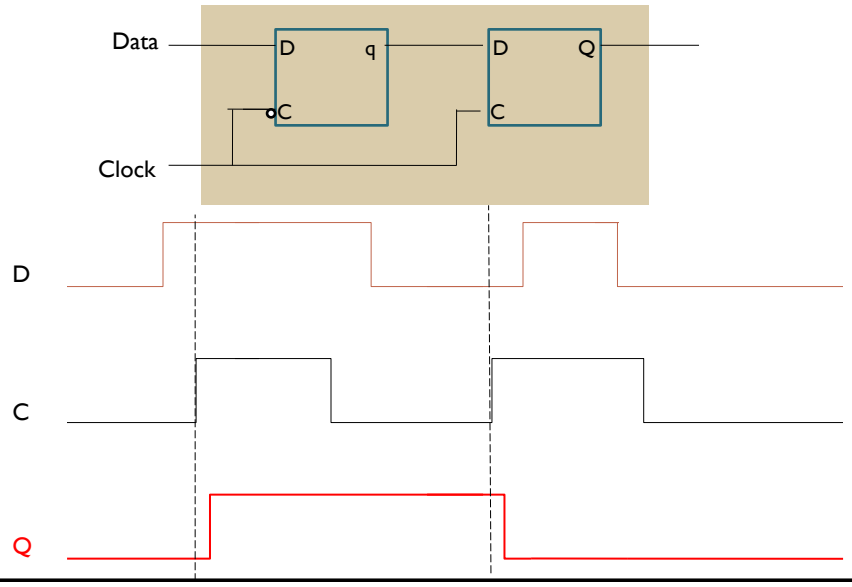
D-Flip Flop (positive edge triggered)



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FF Summary

Flip-Flop Characteristic Table

JK Flip-Flop

J	K	Q^+	Operation
0	0	Q	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q′	Complement

SR Flip-Flop

S	R	Q^+	Operation
0	0	Q	No Change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

D Flip-Flop

D	Q^+	Operation
0	0	Reset
1	1	Set

T Flip-Flop

T	Q^+	Operation
0	Q	No Change
1	Q′	Complement

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