

EE 3613: Computer Organization

Arithmetic for Computers – 2

Carry Look Ahead Adder

Avinash Karanth

Department of Electrical Engineering & Computer Science
Ohio University, Athens, Ohio 45701

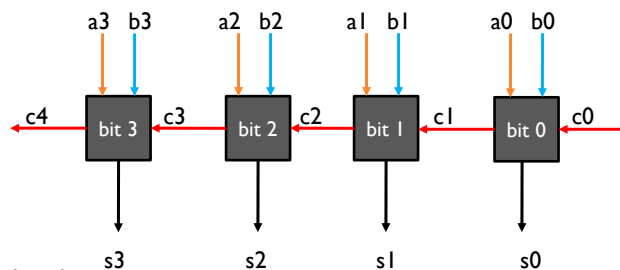
E-mail: karanth@ohio.edu

Website: <http://oucsace.cs.ohiou.edu/~avinashk/ee461a.htm>

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Problem: Ripple Carry Adder is Slow!

- Propagation time of the carry bit takes time – Sequential operation



- $c_{i+1} = a_i b_i + b_i c_i + a_i c_i$
- $s_i = a_i' b_i' c_i + a_i' b_i c_i' + a_i b_i' c_i' + a_i b_i c_i$
- How many gate delays are required for a n -bit sum?
 - $2(n-1) + 3$

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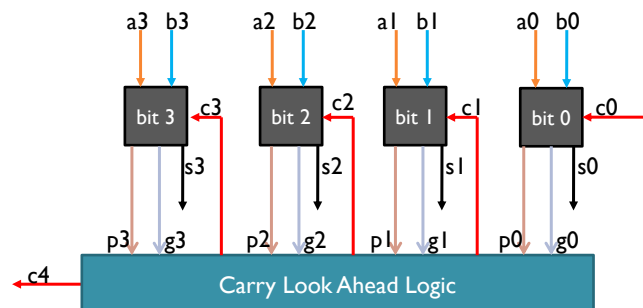
1st Try: Carry Look Ahead (CLA) Adder

- Lets start again
- $c_{i+1} = (b_i \cdot c_i) + (a_i \cdot c_i) + (a_i \cdot b_i)$
 $= (a_i \cdot b_i) + (a_i + b_i) \cdot c_i$
- $c_1 = (a_0 \cdot b_0) + (a_0 + b_0) \cdot c_0$
- $c_2 = (a_1 \cdot b_1) + (a_1 + b_1) \cdot ((a_0 \cdot b_0) + (a_0 + b_0) \cdot c_0)$
- Repeated use of $(a_i \cdot b_i)$ and $(a_i + b_i)$ in the formula
- **Generate (gi) and Propagate (pi)**
- $g_i = a_i \cdot b_i$ [a carry is always generated]
- $p_i = a_i + b_i$ [if $(i-1)^{\text{th}}$ bit has a carry, it will be propagated to $(i+1)^{\text{th}}$ bit]
- $c_{i+1} = g_i + p_i \cdot c_i$

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1st Try: CLA

- $c_1 = g_0 + p_0 \cdot c_0$
- $c_2 = g_1 + p_1 \cdot c_1 = g_1 + p_1 \cdot (g_0 + p_0 \cdot c_0) = g_1 + p_1 \cdot g_0 + p_1 \cdot p_0 \cdot c_0$
- $c_3 = g_2 + p_2 \cdot c_2 = g_2 + p_2 \cdot (g_1 + p_1 \cdot g_0 + p_1 \cdot p_0 \cdot c_0) = g_2 + p_2 \cdot g_1 + p_2 \cdot p_1 \cdot g_0 + p_2 \cdot p_1 \cdot p_0 \cdot c_0$

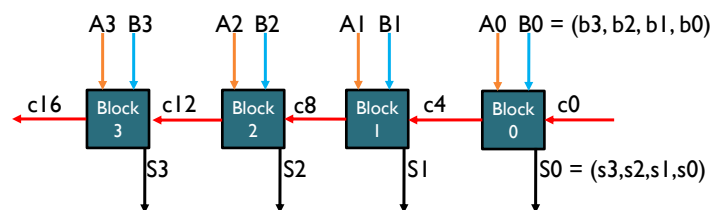


- Number of gate delays for n -bit adder? $(1+2+3 = 6)$
- **Feasible?**

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2nd Try: Two-level CLA

- Combine few bits (say 0, 1, 2 and 3) to generate c_4
- Then ripple it through to the next block (4, 5, 6 and 7) to generate c_8
- Total gate delay for a “n” bit adder = $1 + 2(n/4) + 3$



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3rd Try: 2nd level Generate and Propagate

- $P_0 = p_3.p_2.p_1.p_0$
 - If all 4 bits in a block propagate, the block propagates a carry
- $G_0 = g_3 + p_3.g_2 + p_3.p_2.g_1 + p_3.p_2.p_1.g_0$
 - If atleast 1 bit generates carry and is propagated, the block generates a carry
- $c_4 = (g_3 + p_3.g_2 + p_3.p_2.g_1 + p_3.p_2.p_1.g_0) + (p_3.p_2.p_1.p_0).c_0$
 $= G_0 + P_0.c_0$
- $P_1 = p_7.p_6.p_5.p_4$
- $G_1 = g_7 + p_7.g_6 + p_7.p_6.g_5 + p_7.p_6.p_5.g_4$
- $c_8 = G_1 + P_1.c_4 = G_1 + P_1(G_0 + P_0.c_0)$
 $= G_1 + P_1.G_0 + P_1.P_0.c_0$
- $c_{12} = G_2 + P_2.c_8$
- $c_{16} = G_3 + P_3.c_{12}$
- Total gate delay for a “n” bit adder = $1 + 2 + 2(n/16) + 3$

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Conclusion

- Reducing the gate delays enables faster addition
- Can recursively increase the number of levels from 2 to 3
 - Gate delay?
- Divide and conquer – break into smaller blocks and then ripple (2nd try)
- Or use “SUPER” generates and propagates – (3rd try)