EE 224: INTRODUCTION TO DIGITAL CIRCUITS & COMPUTER DESIGN

Lecture 5: Sequential Logic - 2
Analysis of Clocked Sequential Systems

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Course Administration

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- Hw 2 due on today Monday 4/26
- Hw 3 posted, due on Friday 4/30 by 1:00 PM (drop outside my office)
- Quiz 2 on Wednesday 4/28
- **Exam 1 on Monday 5/3 – syllabus next slide**

Exam 1 - Syllabus

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- Number System and Binary Arithmetic
- Boolean Algebra, Simplification and K-maps
- Combinational Logic (Adders, Muxes, Decoders, PLAs)
- Sequential Logic (Latches and Flip Flops)
- Analysis of Clocked Sequential Logic (Moore and Mealy machines)

FF Summary

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Flip-Flop Characteristic Table

JK Flip-Flop

J	K	Q^+	Operation
0	0	Q	No Change
0	1	0	Reset
1	0	1	Set
1	1	Q'	Complement

SR Flip-Flop

S	R	Q^+	Operation
0	0	Q	No Change
0	1	0	Reset
1	0	1	Set
1	1	?	Undefined

D Flip-Flop

D	Q^+	Operation
0	0	Reset
1	1	Set

T Flip-Flop

T	Q^+	Operation
0	Q	No Change
1	Q'	Complement

FF Transition Input Codes

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- Using FF state tables we can derive the input conditions that will cause specific transitions in each FF output

- 4 possible transitions:
  - D & T FFs have well-defined input conditions in each case
  - J-K FF has 'Don't Care' (X) conditions

- Key to follow sequential logic circuit design examples (i.e. counters)

FF Outputs		FF Inputs		
Q(t)	Q(t+1)	T	D	J-K
0	0	0	0	0-X
0	1	1	1	1-X
1	0	1	0	X-1
1	1	0	1	X-0

FF Excitation Table

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Flip-Flop Excitation Table

JK Flip-Flop

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

SR Flip-Flop

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D Flip-Flop

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip-Flop

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

Analysis by Signal Tracing and Timing Charts

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- Analysis steps:
  - Assume an initial state of FFs (all FFs reset to 0 unless specified)
  - For the input sequence, determine the circuit output(s) and FF inputs
  - Determine the new set of FF states after the next active clock edge
  - Determine the output(s) that corresponds to the new states

Two Types of Clocked Sequential Circuits

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- Moore Machine: If the output of a sequential circuit is a function of the present state only
- Mealy Machine: If the output of a sequential circuit is a function of both the present state and the input

State Tables and Graphs

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- State Table Construction
  - Step 1: Determine the FF input equations and output equations from the circuit
  - Step 2: Derive the next state equation for each FF from input equations from the circuit

D FF: $Q^+ = D$
T FF: $Q^+ = T \oplus Q$
SR FF: $Q^+ = S + R'Q$
JK FF: $Q^+ = JQ' + K'Q$

  - Step 3: Plot a next state map for each FF
  - Step 4: Combine the maps to form a state table

Example of Moore's Machine (1/4)

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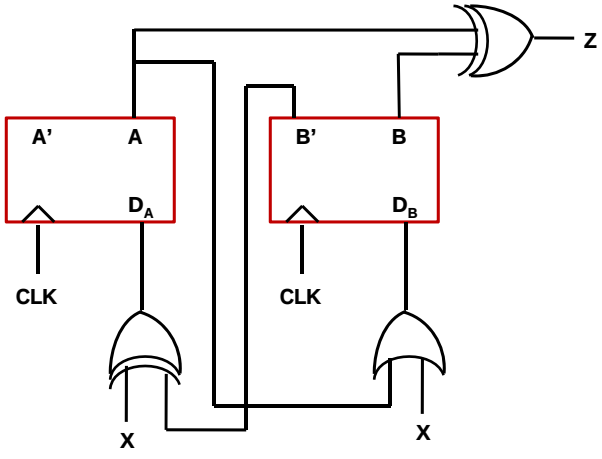

$Z = A \oplus B$

$D_A = X \oplus B'$

$D_B = X + A$

Example of Moore's Machine (2/4)

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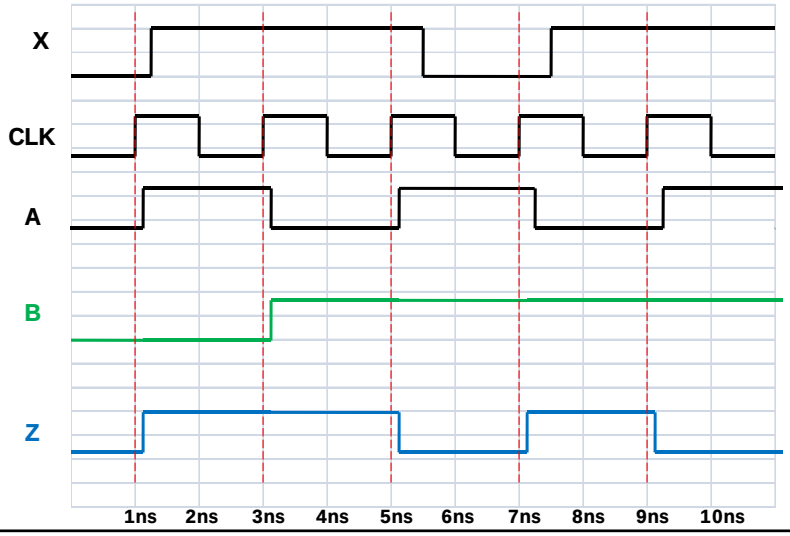
Assume the initial value of A = 0, B = 0, Z = 0



Example of Moore's Machine (3/4)

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- Step 1: FF input equations and output equations:
  - $Z = A \oplus B$ $D_A = X \oplus B'$ $D_B = X + A$
- Step 2: Next state equations for the FF are:
  - $A^+ = X \oplus B'$ $B^+ = X + A$
- Step 3: Corresponding K-maps for A^+ and B^+

AB \ X	0	1
00	1	0
01	0	1
11	0	1
10	1	0

AB \ X	0	1
00	0	1
01	0	1
11	1	1
10	1	1

Example of Moore's Machine (4/4)

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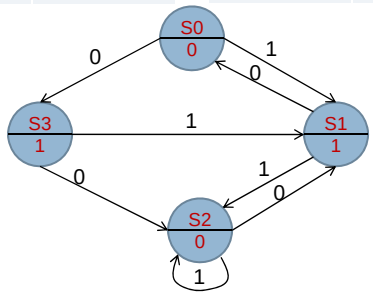
- Step 4: Combine the K-maps into transition table shown here from which states can be derived

AB	A^+B^+ X = 0	X = 1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

Present State	Next State X = 0	X = 1	Present Output (Z)
S0	S3	S1	0
S1	S0	S2	1
S2	S1	S2	0
S3	S2	S1	1



Example of Mealy Machine (1/4)

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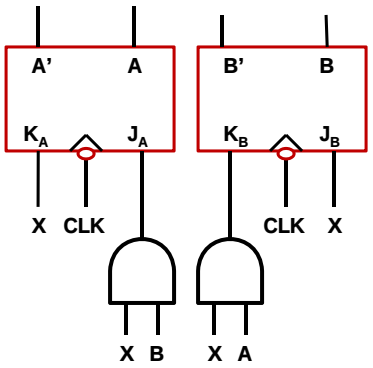

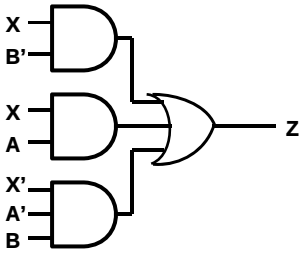

$A^+ = J_A A' + K_A' A = XBA' + X'A$

$B^+ = J_B B' + K_B' B = XB' + (AX)'B = XB' + X'B + A'B$

$Z = X'A'B + XB' + XA$

Example of Mealy Machine (2/4)

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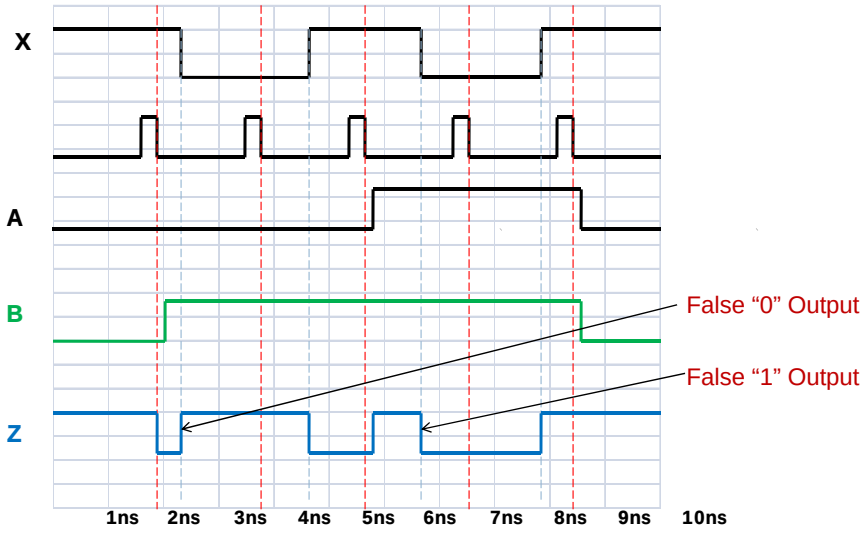

Example of Mealy Machine (3/4)

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- Step 1: FF input equations and output equations:
  - $J_A = XB$, $K_A = X$ $\quad\quad$ $J_B = X$, $K_B = XA$
- Step 2: Next state equations for the FF are:

  $A^+ = XBA' + X'A$

  $B^+ = XB' + X'B + A'B$

  $Z = X'A'B + XB' + XA$
- Step 3: Corresponding K-maps for A^+ B^+ and Z

AB \ X	0	1
00	0	0
01	0	1
11	1	0
10	1	0

AB \ X	0	1
00	0	1
01	1	1
11	1	0
10	0	1

AB \ X	0	1
00	0	1
01	1	0
11	0	1
10	0	1

Example of Mealy Machine (2/4)

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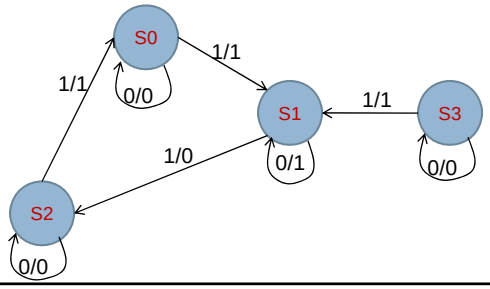
- Step 4: Combine the K-maps into transition table shown here from which states can be derived

AB	A^+B^+ X = 0	X = 1	Z X = 0	X = 1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

Present State	Next State X = 0	X = 1	Present Output (Z) X = 0	X = 1
S0	S0	S1	0	1
S1	S1	S2	1	0
S2	S2	S0	0	1
S3	S3	S1	0	1



Design of a Sequence Detector (1/3)

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- Circuit examines a string of 0's and 1's applied to X input and generates an output Z = 1 only when the prescribed sequence occurs with the assumption that X can only change between clock cycles. Design the circuit so that the input sequence ending in 101 will produce an output Z = 1 coincident with the last 1. The circuit does not reset when a 1 occurs.

```
X = 0 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0
Z = 0 0 0 0 0 0 1 0 0 0 0 0 1 0 1 0 0
```

- Is this a Mealy machine or Moore machine?

Design of a Sequence Detector (2/3)

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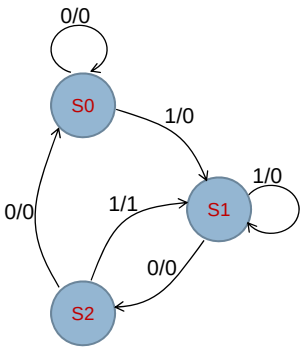

Present State	Next State X = 0	Next State X = 1	Present Output (Z) X = 0	Present Output (Z) X = 1
S0	S0	S1	0	0
S1	S2	S1	0	0
S2	S0	S1	0	1

AB	A^+B^+ X = 0	A^+B^+ X = 1	Z X = 0	Z X = 1
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

Design of a Sequence Detector (3/3)

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AB \ X	0	1
00	0	0
01	1	0
11	X	X
10	0	0

AB \ X	0	1
00	0	1
01	0	1
11	X	X
10	0	1

AB \ X	0	1
00	0	0
01	0	0
11	X	X
10	0	1

$A^+ = X'B$

$B^+ = X$

$Z = XA$

How about Moore Machine?

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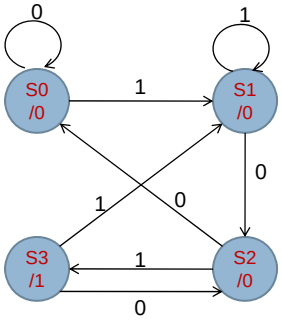

Present State	Next State X = 0	Next State X = 1	Present Output (Z)
S0	S0	S1	0
S1	S2	S1	0
S2	S0	S3	0
S3	S2	S1	1

AB	A^+B^+ X = 0	A^+B^+ X = 1	Z
00	00	01	0
01	11	01	0
11	00	10	0
10	11	01	1

Complex Design - 1

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- The output Z = 1 if the input sequence ends in either 010 or 1001 and Z should be 0 otherwise. Here's a typical sequence

X = 0 0 1 0 1 0 0 1 0 0 0 1 0 0 1 1 0

Z = 0 0 0 1 0 1 0 1 1 0 0 0 1 0 1 0 0

Solution - 1

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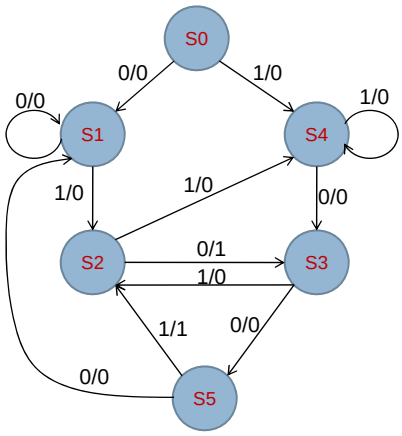

State	Sequence Ends In
S0	Reset
S1	0 (but not 10)
S2	01
S3	10
S4	1 (but not 10)
S5	100

Complex Design - 2

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- A sequential circuit has one input (X) and two outputs (Z1 and Z2). An output Z1 = 1 occurs every time when the input sequence 100 is completed, provided that the sequence 010 has never occurred. An output Z2 = 1 occurs every time the input sequence 010 is completed. Note that once Z2 = 1 output has occurred, Z1 = 1 can never occur but not vice versa. Find a mealy state graph and table.

X	=	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0	0
Z1	=	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Z2	=	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0	0	0	0	1	0

Solution - 2

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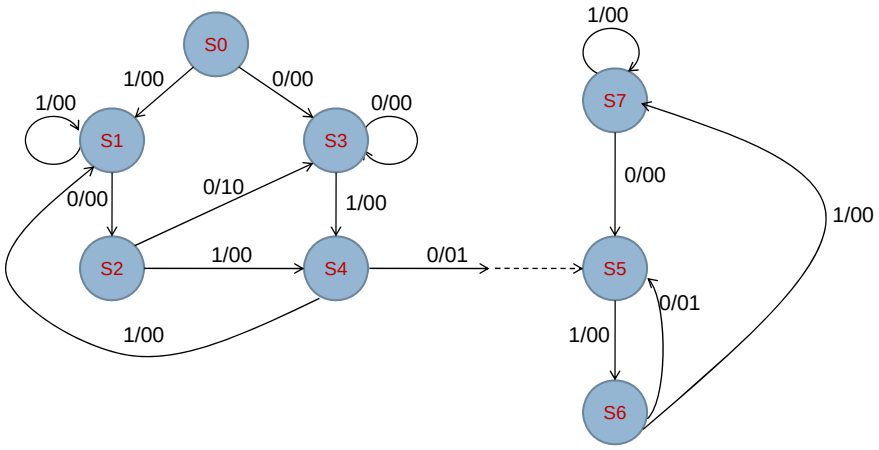

Complex Design - 3

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- A sequential circuit has two inputs (X1 and X2) and one output Z. The output remembers the constant value unless one of the following input sequence occurs:
  - The input sequence X1 X2 = 01, 11 causes the output to become 0
  - The input sequence X1 X2 = 10, 11 causes the output to become 1
  - The input sequence X1 X2 = 10, 11 causes the output to change value (toggle)

Solution 3 (see text for complete solution

Previous Input	Output (Z)	State Designation
00 or 11	0	S0
00 or 11	1	S1
01	0	S2
01	1	S3
10	0	S4
10	1	S5