Department of Electrical Engineering and Computer Science
Ohio University, Athens, Ohio.

Course Syllabus
Fall 2011 EE 102: Introduction to Computer Engineering

Course Information

Credits: 4

Class Location: ARC 102
Class Days (all sections): M,W,F
Class Time: 4:10 - 5:00 PM

Lab Location: Stocker Engineering Building STKR 314
Section 101: Wednesday 1:10 - 3:00 PM
Section 102: Thursday 3:10 - 5:00 PM
Section 103: Tuesday 2:10 - 4:00 PM

Course Instructor Information

Name: Avinash Kodi
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Phone: (740)-597-1481
E-mail: kodi@ohio.edu
Webpage: http://oucsace.cs.ohiou.edu/∼avinashk/classes/ee102/ee102.htm
Office Hours: 10:00 AM - 12:00 PM Monday, Friday, or by appointment

Textbook

- (Required) Charles H. Roth, *Fundamentals of Logic Design* - 6th Edition, Brooks/Cole 2010.
- (Optional) M.M. Mano & C.R. Kime, *Logic and Computer Design Fundamentals*, 4th Edition, Prentice-Hall, 2008.

Prerequisites

- MATH 113 or above or PLCMNT LVL 2 or higher

Class Policies

- **Attendance**: Class attendance is required. If you will need to miss class for some reason, you should contact your instructor in advance to determine the consequences of missing class. Please note that while textbook is a reference, many problems and exercises will be discussed in class.
- **Academic Misconduct**: Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor, all course work should be done on your own. Any exceptions to this could result in an "F" for the course. Please refer to the OU Student Code of Conduct.

- **Reading**: Be prepared. Read over the material before class and laboratory. For the most part lecture will follow mostly the organization of the book. I will do my best to post upcoming lecture topics, when necessary. Check the class webpage regularly for announcements.

- **Homeworks**: Homework exercises will be assigned throughout the term to assist you in mastering the basic course concepts. It is strongly encouraged that any student having difficulty with homework assignments come to office hours or email the instructor with questions. No late homework assignments will be accepted due to the tight schedule. Please contact the instructor in case of emergencies.

- **Quizzes**: There will be atleast 4 in-class pop quizzes in this course. These will be closed book quizzes. These quizzes will be conducted throughout the quarter to demonstrate your understanding of lectures and homeworks. There will be no makeup quizzes.

- **Exams**: We will have three exams (two Midterms and one Final) in this course to give you the opportunity to show that you have mastered the knowledge and skills addressed. Two midterm exams have the same weight and cover roughly two halves of the course work, while the final exam is based on all classwork including the lab modules.

- **Laboratory**: The teaching assistant for EE 102 for the Fall 2011 quarter is Mr. Brian Neel, a graduate student in the EECS department (**bn179706@ohio.edu**). In the laboratory you will be expected to record your observations and results on prepared lab sheets. *Students must inform the instructor ahead of time regarding absence from lab when possible, and all missed labs must be made up by the end of the following week.* Lab partners are chosen at random weekly so it is up to the student to become self-sufficient in the laboratory. All students must check the course webpage for laboratory handouts and write-up sheets prior to coming to class. Many of the labs require preliminary work before coming to the lab session, and this pre-laboratory work will be checked before the start of the lab. All lab write-ups are due the following week during the regular lab session.

Grading Policy

Homeworks : 20%
Quizzes : 20%
Midterms (2) : 20%
Final Exam : 20%
Laboratory : 20%

Laboratory 20%

Attendance/Preparedness : 20%
Lab Performance/Results : 40%
Lab Write-up : 40%

- All grades will be posted on Blackboard.

- All grading is based on the 12-point system. [100-93] A, [92-90] A-, [89-87] B+, [86-83] B, [82-80] B-, [79-77] C+, [76-73] C, [72-70] C-, [69-67] D+, [66-63] D, [62-60] D-, [59-..] F. Instructor reserves the right to lower the limits above, but I promise not to raise them.

Course Outline

The goal of this course is to introduce students to the field of computer engineering, in particular, the fundamentals of digital logic design. Students will develop knowledge of the fundamentals of Boolean algebra, binary arithmetic, characteristics of logic gates, flip-flops and basic logic circuits. Furthermore, students will develop an awareness of abstraction, computer organization, and software used for the simple digital circuit simulation. Lab work provides hands-on experience with digital systems.

Course Outcomes

The primary student outcomes desired for this course listed by topic are:

- Information and data Representation
  - an ability to express numbers in decimal, binary, and hexadecimal formats
  - an ability to represent characters with ASCII notation with and without parity
  - an understanding of binary numbers
- Computer Organization Introduction
  - an understanding of hierarchical design principles
  - an understanding of a generic microprocessor architecture
- Computer Arithmetic
  - an ability to perform binary arithmetic
- Boolean Algebra
  - an understanding of the basic operations and law of Boolean algebra
  - an ability to construct a truth table for a Boolean expression
  - an understanding of the minterms and maxterms of a Boolean algebraic expression
- Combinational Logic
  - an ability to implement a Boolean algebraic expression with digital logic gates
  - an understanding of digital logic
- Sequential Logic
  - an ability to construct a timing diagram for a digital system
  - an ability to implement basic synchronous sequential circuits with flip-flops
  - an ability to derive the state table diagram from a sequential circuits
- Digital Devices
  - an understanding of the operation of logic gates

  - an understanding of the operation of SR, T, JK, and D flip-flops
  - an understanding of the operation of counters and registers
  - an understanding of the operation of multiplexers, decoders and ROM
- Software Introduction
  - a knowledge of the basic circuit simulation software
- 102 Lab
  - an ability to experimentally validate a theoretical property
  - a knowledge of IC pin numbering
  - an ability to coordinate circuit simulation with hardware results
- Workplace Diversity Introduction
  - an ability to listen to different opinions about diversity
  - an ability to work successfully with people from different cultural backgrounds

Tentative Schedule

Week 1: Introduction, Binary Arithmetic - No Lab
Week 2: Boolean Algebra - Introduction to IDL 800 Digital Lab
Week 3: Boolean Algebra - Basic Logic Gates
Week 4: Karnaugh Maps - Simulation: Electronic Workbench
Week 5: Combinational Logic Design - Logic Implementation
Week 6: Combinational Logic Design - Hierarchical Design
Week 7: Combinational Logic Design - Arithmetic Functions
Week 8: Sequential Logic Design - Sequential Logic
Week 9: Sequential Logic Design - Registers
Week 10: Sequential Logic Design - Counters

Tentative Dates

Midterm 1: October 3, 2011 (in-class)
Midterm 2: November 2, 2011 (in-class)
Final Exam: November 21, 2011 (2:30 PM - 4:30 PM)